BMBAD BJESR Mühendislik Bilimleri ve Araştırmaları Dergisi
Journal of Engineering Sciences and Researches

A Reconfigurable 4th Order IIR Filter For The Low Frequency Applications

Düşük Frekans Uygulamaları İçin Yeniden Yapılandırılabilir Bir IIR Süzgeç Yapısı

[1]Deniz OZENLİ

[1]Department of Electronics Engineering, Turkish Air Force Academy, National Defence University, Istanbul, 34149 TURKEY

[1]dozenli@hho.msu.edu.tr

Araştırma Makalesi/Research Article

ARTICLE INFO

Article history

Received : 13 May 2023
Accepted : 30 June 2023

Keywords:

Infinite Impulse Response (IIR), IIR filter,Z-Transform, Verilog.

ABSTRACT

Huge numbers of advanced electrical engineering applications employ infinite impulse response (IIR) filters very frequently in order to meet market's demands. Especially, some applications such as video processing, digital signal processing and high-speed digital communication require computational efficiency and low latency. In this point of view, high-speed processing of digital data requires a digital signal processor or an FPGA instead of a conventional microprocessor. This work gives a FPGA hardware design of a 4th order IIR reconfigurable filter structure. The proposed filter's maximum clock frequency is around 32MHz which covers different low frequency applications from biomedical signal processing up to speech applications. To verify the performance of the filter, 4th order Butterworth and Chebyshev filters are realized in the basis of MATLAB results and FPGA behavioral model. It should be considered that the proposed filter scheme presents promising results to meet low frequency applications.

MAKALE BİLGİSİ

Makale Tarihleri

Gönderim : 13 Mayıs 2023
Kabul : 30 Haziran 2023

Anahtar Kelimeler:

Sonsuz Uzunluklu Birim Dürtü Yanıtı (IIR), IIR Süzgeç, Z-Dönüşümü, Verilog.

ÖZET

Çok sayıda ileri elektrik mühendisliği uygulaması, tüketici taleplerini karşılamak adına çok sık olarak sonsuz dürtü yanıta sahip (IIR) filtreleri bünyelerinde barındırırlar. Özellikle video işleme, sayısal işaret işleme ve yüksek hızlı sayısal iletişim gibi bazı uygulamalar, hesaplama verimliliği ve düşük gecikme süresi gerektirir. Bu noktada, sayısal verilerin yüksek hızda işlenmesi, geleneksel bir mikroişlemci yerine bir sayısal işaret işlemcisi veya bir FPGA gerektirir. Bu çalışmada 4.dereceden IIR ayarlanabilir bir süzgeç yapısı FPGA donanım tasarımı eşliğinde verilecektir. Önerilen süzgecin maksimum saat frekansı 32MHz civarındadır ki, bu frekans biyomedikal işaret işlemeden konuşma işareti işlemeye kadar pek çok uygulamaya uygun aralıktadır. Süzgecin başarımını doğrulamak adına 4.dereceden Butterworth ve Chebyshev süzgeç örnekleri MATLAB ve FPGA davranışsal modelleri kıyaslaması tabanında sunulmaktadır. Şu ifade edilebilir ki önerilen süzgeç yapısı düşük frekans uygulamalarında yer alabilmek adına güvenilir sonuçlar içermektedir.

ORCID ID: [1]0000-0002-6381-3629

1. INTRODUCTION

In advanced signal processing, a great deal of filtering applications have been realized by employing digital signal processing blocks. In this view, analog to digital conversion is employed, which contains sampling and quantizer circuitries. After conversion, digital filtering can be provided by using different units such as microprocessor units (MCUs), digital signal processors (DSPs) or FPGAs. In this manner, Figure 1 illustrates a low frequency signal acquisition flow based on digital filtering. In the end of filtering, baseband signal can be safely converted back to the analog domain in order to communicate with the other parts in the medium. It should be noted that real time performance and total design time are crucial parameters for the digital signal processing. Hence, FPGA based operations can be safely preferred in order to reduce the design cycles and increase real time performance to meet market's demands [1-3].

Most of digital signal processing applications necessitate a resilient digital filter block based on low cost, less memory and low power design strategy. In the further view of digital filters, FIR and IIR architectures are presented in the previous studies [4-11]. When compared to the FIR counterparts, IIR filter structures presents more flexibility, less memory requirement and reduced design time. Also, they bring some drawbacks such as non-linear phase characteristics and complicated feedback mechanism worsening system stability. On the other hand, in order to discard noisy signal components placed in high frequency region, fast and more stable IIR digital filters are implemented in basis of behavioral models and generated special filter functions such as Chebyshev or Butterworth.

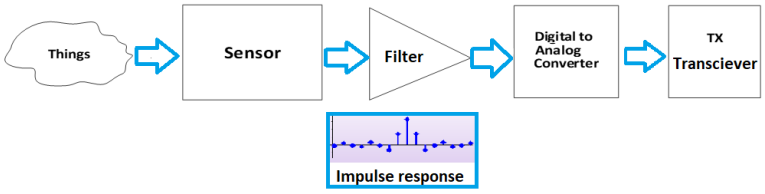


Figure 1. Low frequency signal acquisition system in digital signal processing.

Whereas FIR filters bring several advantages such as linearity, stability and fixed-point analysis, IIR architectures can be safely implemented in different low frequency applications ranging from biomedical filtering up to speech analysis and recognition. In addition, FIR filters have high computational burden and memory requirements. In this view, some FIR structures necessitate huge amount of design time compared to IIR counterparts. In order to decrease design cycles, there are some commercial software tools in the market such as MATLAB and Simulink programs presenting user friendly design tools, which the designer can define a cost function and filter constraints. In the further view, Verilog HDL (Hardware Description Language) gives new opportunities to the users based on high level design paths. Therefore, behavioral view of the desired filter architecture can be safely transformed into block level synthesis, which will be resulted in transistor level design by adding pads and clock trees [12-13].

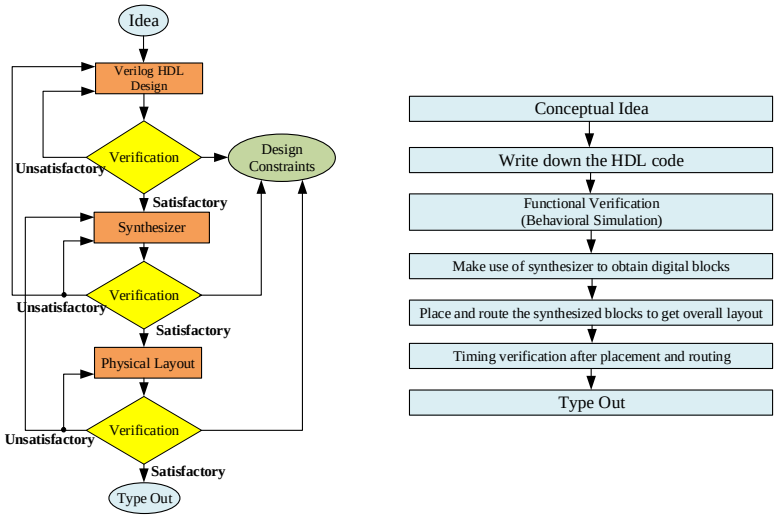
In this paper, 4^{th} order IIR filters including Butterworth and Chebyshev architectures are presented by using Transpose design technique [13]. Normalized filter frequency is selected from 0.1 up to 0.6, which is suitable for biomedical and speech applications. In order to evaluate the filter performance, MATLAB results are compared with Verilog based design. In addition, design flow of the architectures is given with device utilizations after synthesis of the core 4^{th} order reconfigurable IIR filter. To justify the performance, real audio (speech) signal is sampled at 48kHz and summed with additive gaussian noise. The filtered output signal is evaluated in both of time and frequency domains.

This paper is organized as follows: The next chapter gives the design flow of the proposed 4^{th} order IIR filter architecture. The third part introduces Verilog implementation of the filter, whereas fourth chapter gives the filter results in comparison with MATLAB ideal responses. The last part ends up the paper with concluding remarks.

2. THE PROPOSED 4^{TH} ORDER IIR FILTER DESIGN METHODOLOGY

Low-pass and high-pass filters allow signals in pass-band region, whilst the other signals outside the pass-band region are suppressed with high rejection ratio. In this work, low-pass and high-pass filters in basis of Butterworth and Chebyshev structures are generated. It should be noted that Butterworth structure gives maximally flatness in pass-band, whereas Chebyshev topology has an equiripple amplitude response [14]. Furthermore, the digital filters can be designed in FIR or IIR topology. In order to reduce memory requirement and effects arising from windowing steps, IIR configuration is preferred in this work. General IIR filter design strategy can be given in Figure 2, whilst (1) and (2) give IIR difference equation.

In this work, sampling frequency f_s is selected as 48kHz, when low-pass and high-pass filters are designed. While designing the filters, analog transfer function of $H(s)$ is converted to $H(z)$ by using bilinear transformation [15-16]. Hence, (3) and (4) are applied to the desired filters in order to obtain the projection of the filters in unit circle. It should be considered that the designed filters in this work are 4^{th} order, also have four zeroes and poles on the unit circle. In this respect, a_k and b_k coefficients can be obtained for each IIR filter configurations.



a) b)

Figure 2. General IIR filter design strategy: a) Design flow, b) Details in each design step up to production.

$$y(n) = \sum_{k=0}^{M} b_k x(n-k) - \sum_{k=0}^{N} a_k y(n-k) \tag{1}$$

$$H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{\sum_{k=1}^{N} a_k z^{-k}} \tag{2}$$

$$s = \frac{2}{T_s} \cdot \frac{1-z^{-1}}{1+z^{-1}} \tag{3}$$

$$z = r.e^{j\omega} = \frac{1+\frac{T_s}{2}s}{1-\frac{T_s}{2}s} \tag{4}$$

When considered re-arrangements described in (3)-(4), the filter coefficients can be employed in transposed IIR filter topology as illustrated in Figure 3. In order to provide low-pass and high-pass filters, Butterworth and Chebyshev concepts are employed. For 16 bits resolution level and fixed design methodology, impulse and step responses are given in Figure 4 for the Butterworth 4th order low-pass filters with 0.1 normalized cut-off frequency Moreover, Figures 5, 6 and 7 give low-pass and high-pass filter-time responses according to the 4th order Chebyshev filter design with different normalized cut-off frequencies.

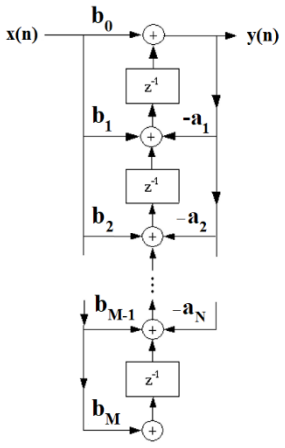
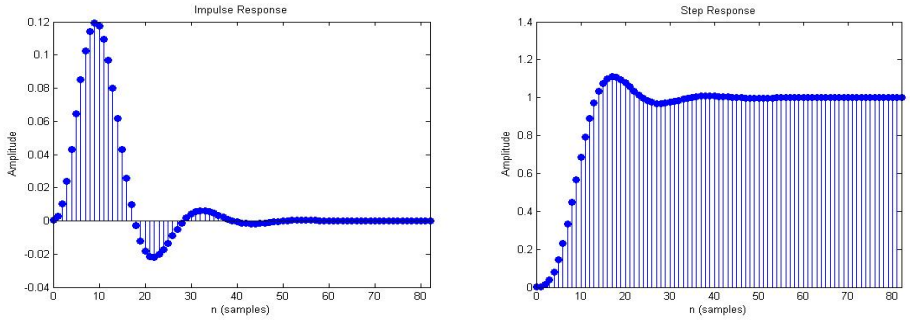
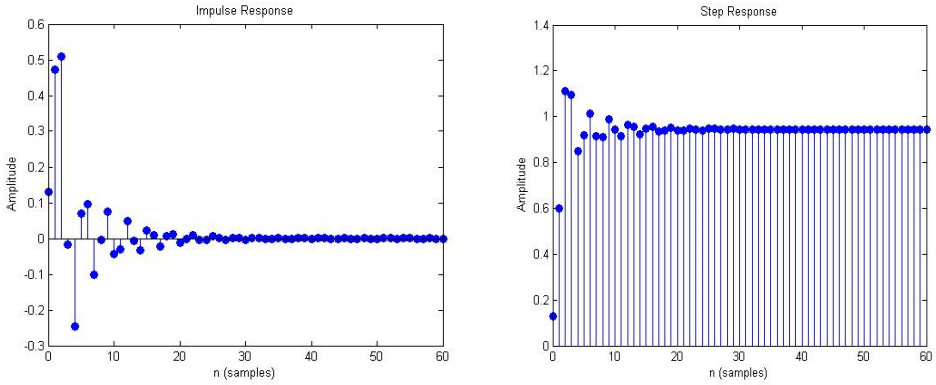


Figure 3. Transposed IIR filter realization.



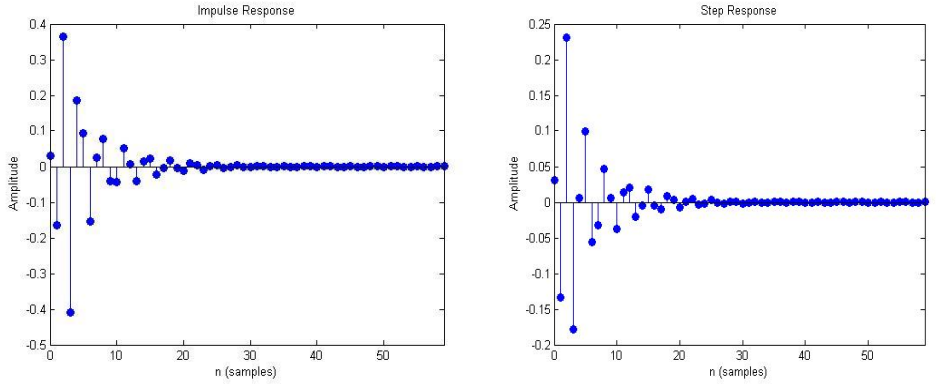
a) b)

Figure 4. Butterworth 4th order low-pass filter with 0.1 normalized cut-off frequency: a) Impulse response, b) Step response.



a) b)

Figure 5. Chebyshev 4th order low-pass filter with 0.6 normalized cut-off frequency: a) Impulse response, b) Step response.



a) b)

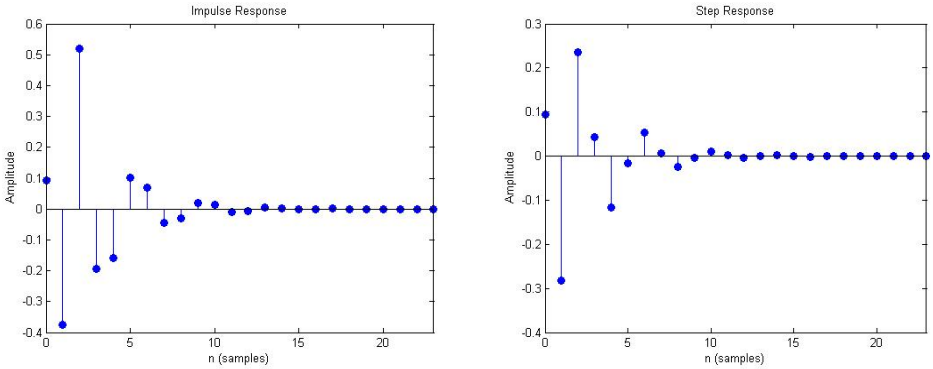
Figure 6. Chebyshev 4th order high-pass filter with 0.6 normalized cut-off frequency: a) Impulse response, b) Step response.

3. VERILOG IMPLEMENTATION OF THE PROPOSED FILTER

In order to realize the proposed filter structure, a design flow is employed as illustrated in Figure 8. After description of filter type (FIR/IIR, order of filter or Chebyshev/Butterworth/Elliptic topologies etc.), transposed filter structure is constructed in behavioral simulation. In conjunction with the algorithm in Table 1 and design flow in Figure.8, transposed IIR filter is implemented. Also, filter coefficients determine the transposed filter structure's forward and reverse path gains. In this respect, the coefficients are given for all configurations of the proposed 4th order IIR structure in Table 2. After the filter coefficients are obtained, which result in the desired filter response, behavioral simulation is generated in order to testify the filter responses.

As shown in Figure 9, behavioral simulation is given in order to obtain transposed 4th order IIR filter structure signal flow. In this graph, filter output is investigated with regard to each filter configuration. Also, it can be

verified that filter output is generated correctly based on delay cells and gain blocks in each positive edge of the clock signal. In this respect, the filter responses of each configuration can be compared with the theoretical results after filter results are saved in a separate file.



a) b)

Figure 7. Chebyshev 4th order high-pass filter with 0.5 normalized cut-off frequency: a) Impulse response, b) Step response.

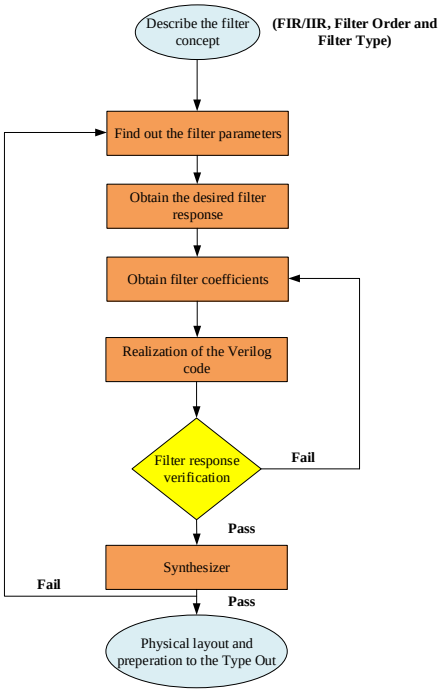


Figure 8. 4th order IIR filter design flow in Verilog.

Table 1. Behavioral design of the 4th order IIR filter in Verilog.

Algorithm: Discrete Time 4th Order IIR Filter
1: Define filter inputs
2: Define inputs to be activated in positive edge of the clock
3: Output assignment in 16 bits in the end of filtering block
4: Entering the pre-determined filter coefficients
5: 4th order IIR filter construction in transposed architecture
6: Non-blocking assignments for the filter's output calculation in each positive edge of the clock signal

After investigation of filter responses in the behavioral simulations, RTL view of the designed filter block can be obtained by using synthesizer. Therefore, top view of the designed filter block can be given as Figure 10a, whereas the estimated number of utilized logic blocks can be tabulated in Table 2. All logic blocks, which consist of delay cells and multiplexers can be depicted as shown in Figure 10a 10b and 10c. In this figure, upper and lower parts of the synthesized filter are given separately in order to illustrate logical blocks and interconnections.

Table 2. Filter coefficients of the proposed 4th order IIR filter in the transposed structure illustrated in Figure.3.

4th Order IIR Filter Coefficients		
Filter Configuration	**a**	**b**
Butterworth LP (Normalized f_c =0.1)	[1.0000 -3.1806 3.8612 -2.1122 0.4383]	[0.0004 0.0017 0.0025 0.0017 0.0004]
Chebyshev LP (Normalized f_c =0.6)	[1.0000 0.3516 0.7708 -0.0614 0.1299]	[0.1293 0.5171 0.7756 0.5171 0.1293]
Chebyshev HP (Normalized f_c =0.6)	[1.0000 1.3834 1.4721 0.8012 0.2286]	[0.0304 -0.1218 0.1827 -0.1218 0.0304]
Chebyshev HP (Normalized f_c =0.5)	[1.0000 0.0000 0.4860 0.0000 0.0177]	[0.0940 -0.3759 0.5639 -0.3759 0.0940]

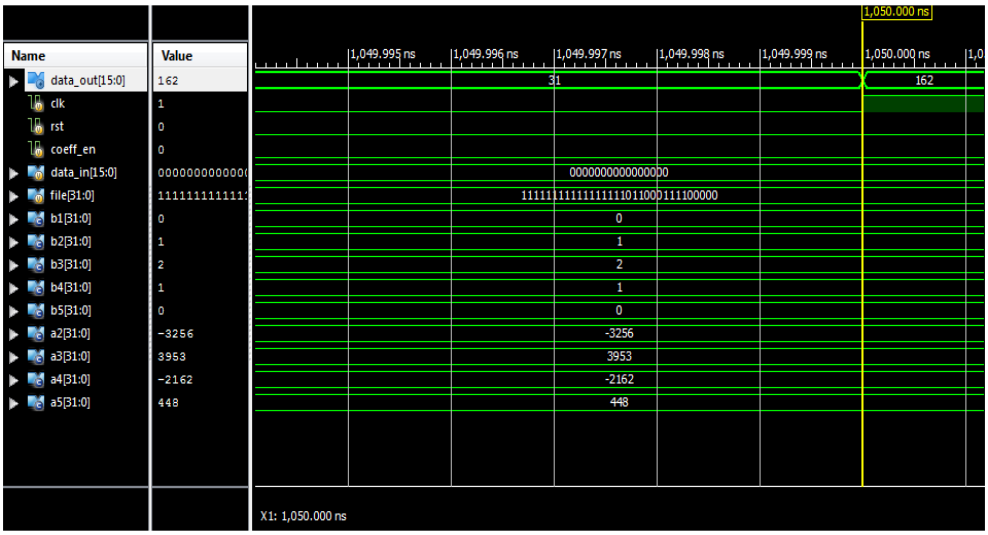
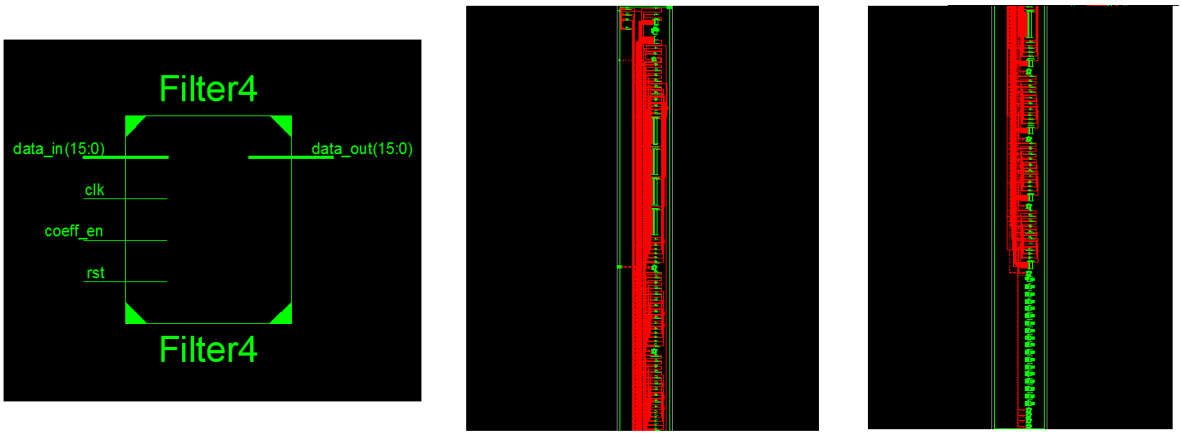


Figure 9. The proposed IIR filter structure's behavioral simulation in timescale of 1ps. (Clock Frequency is selected as 1MHz.).



a) b) c)

Figure 10. The proposed IIR filter's register transfer level (RTL) view with synthesized logic blocks: a) Top view, b) Upper side of the core structure, c) Lower side of the core structure.

When considered estimated logical blocks' utilization given in Table 3, synthesizing of the filter structure is finalized without any errors. Meanwhile, it should be noted that the number of slices is more than available slices in ISE 13.4 design suite. This is because the required number of slices is likely to be more than available slices. If type out of the filter structure is considered after place and route process, total chip area can be increasing due to additional transistors and logical blocks in order to reach the required number of slices. Moreover, maximum clock frequency of the designed IIR filter structure is given as 32MHz, whereas combinational path delay is around of 18ns. The maximum clock frequency enables the filter structure to be a competitive candidate for the low frequency applications up to around of 1.5MHz, which are ranging from biomedical filtering to speech processing implementations.

Table 3. The proposed IIR filter's logic blocks utilization (Estimated by Xlinx Verilog Design Suite version of ISE 13.4).

Device Utilization Summary (Estimated Values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1077	768	140%
Number of Slice Flip- Flops	306	1536	19%
Number of 4 input LUTs	1536	1841	84%
Number of bonded IOBs	35	63	55%
Number of MUX 18x18s	4	4	100%
Number of GCLKs	1	8	12%

4. VERIFICATION OF THE PROPOSED ARCHITECTURE

In order to verify performance of the IIR filter structure, ideal filter characteristics should be compared with FPGA behavior compiled with the transposed topology aforementioned in the previous section. In this analysis, ISE 13.4 design environment is employed with SPARTAN-3 FPGA development board. Also, codes are executed by 64-bit Intel i5 processor, running at 2.4GHz. In this respect, provided IIR filter results can be justified for each configuration with sampling frequency of 48kHz. When considered gain frequency responses of the filter configurations shown in Figure 11, FPGA results are in a good accordance with the ideal behavior. As for the suppression bands of the filters, there are no high rejection ratios due to fact that filter coefficients are quantized with the accuracy of 16 bits. It should be noted that digital filters such as Butterworth, Chebyshev structures or low order FIR structures suffer from the low rejection ratios in the suppression bands. At the expense of increasing filter's order and design complexity, suppression bands' behaviors come closer to the ideal ones.

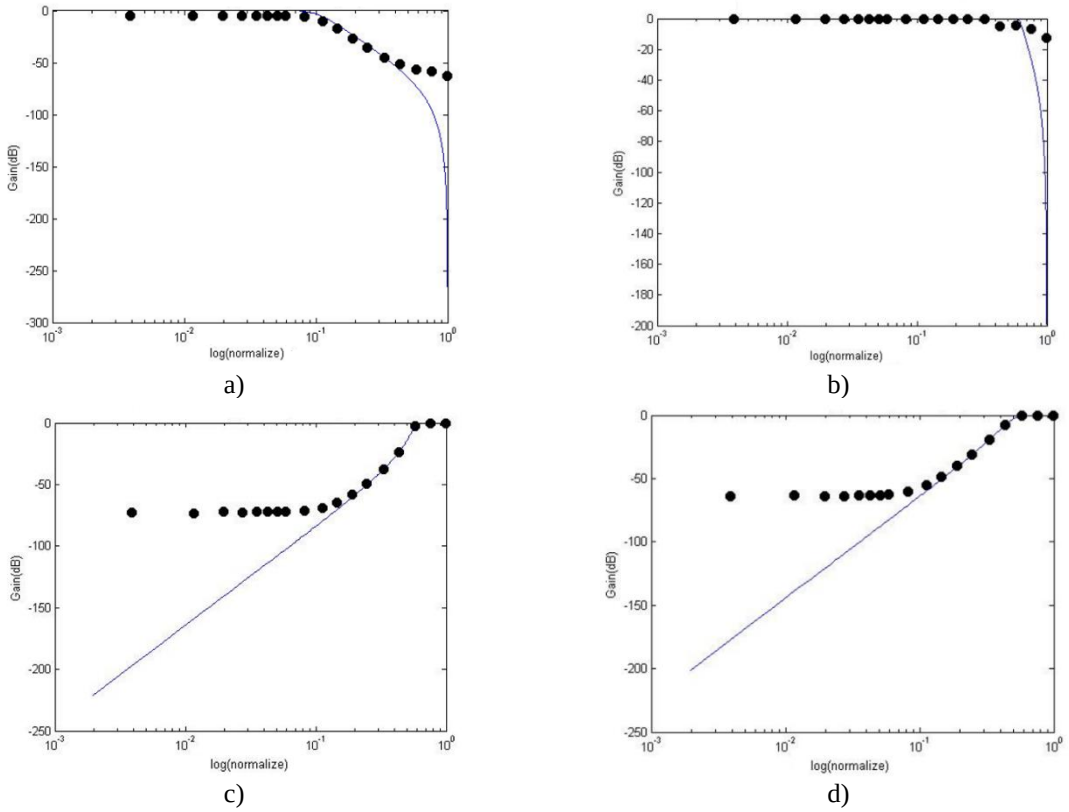


Figure 11. The proposed IIR filter's frequency responses (Solid is ideal response, whereas dots are FPGA results): a) Butterworth 4th order low-pass filter with 0.1 normalized cut-off frequency, b) Chebyshev 4th order low-pass filter with 0.6 normalized cut-off frequency, c) Chebyshev 4th order high-pass filter with 0.6 normalized cut-off frequency, d) Chebyshev 4th order high-pass filter with 0.5 normalized cut-off frequency.

In order to justify the filter's performance, real audio (speech) signal is sampled at 48kHz and summed with additive gaussian noise. In the end of this process, the high frequency noise components are added to the original (clean) signal under the gaussian noisy channel with zero mean and sigma value of 0.05. As shown in Figure 12

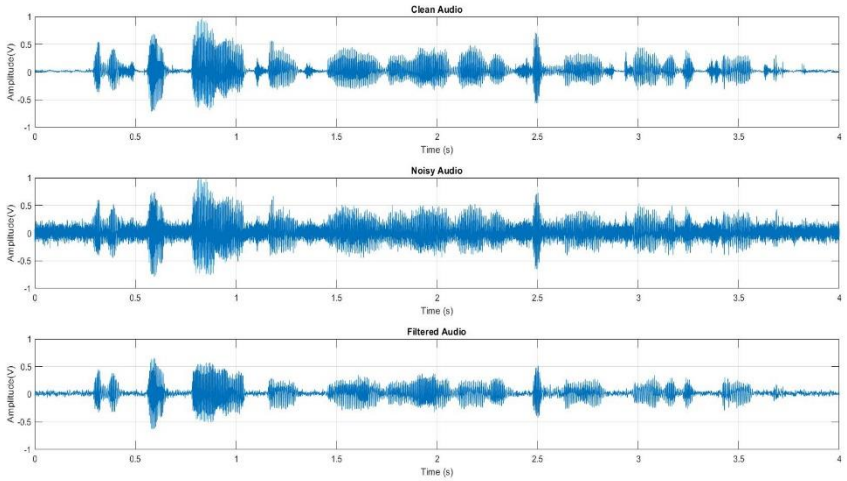


Figure 12. Real Audio signal test for the IIR filtering performance. Upper side: Clean Audio Signal, Center: Noisy Audio Signal Generated with Additive Gaussian Noise Channel, Lower side: Filtered Audio Signal.

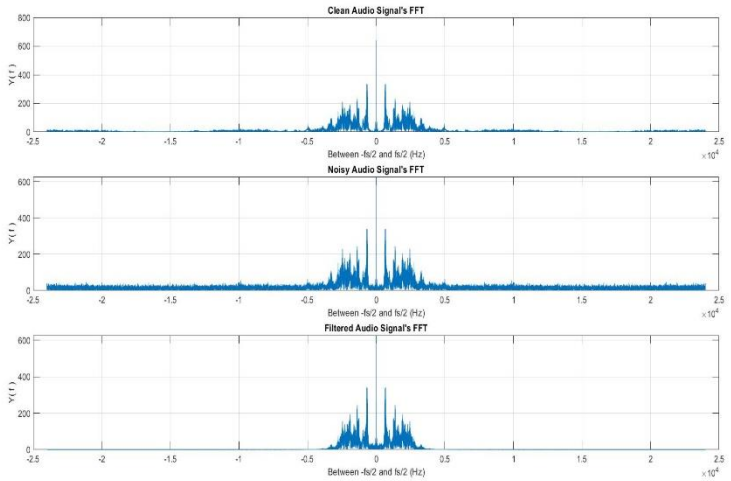


Figure 13. Real Audio signal test for the IIR filtering performance with FFTs. Upper side: Clean Audio Signal's FFT, Center: Noisy Audio Signal's FFT, Lower side: Filtered Audio Signal's FFT.

and Figure 13, noise effects, which are spread over large frequency interval can be removed safely by using the proposed IIR filter structure. It should be noted that in this exemplary acquisition, 4th order Butterworth low-pass filter is employed with 0.1 normalized cut-off frequency as mentioned in the previous section. In order to prove the competitive performance, Table.4 is given in comparison to the previous studies. Hence, it should be noted that the proposed reconfigurable filter structure can be a good candidate for the low frequency applications, where digital signal processing blocks are needed. In the comparison of tabulated resource utilization, the proposed work brings new facilities to the designers in order to decrease the number of multiplexers, memory devices and flip-flops in the digital filtering applications where chip area occupation and calculation efficiency are very crucial.

Table 4. Used FPGA resources in comparison with the previous studies

FPGA Resource Utilization	[4]	[9]	[16]	The Proposed Work
Number of Slice Flip- Flops	1553	896	177	**306**
Number LUTs	4458	896	1662	**1536**
Number of Block RAMs	0	0	2	**0**
Number of MUX	24	0	142	**4**

5. CONCLUSIONS

This work gives a FPGA hardware design of a 4th order IIR reconfigurable filter structure. The proposed filter's maximum clock frequency is around 32MHz which covers different low frequency applications from biomedical signal processing up to speech applications. To verify the performance of the filter, 4th order Butterworth and Chebyshev filters are realized in the basis of MATLAB results and FPGA behavioral model. Also, consumed logic gates and blocks are given with estimated numbers in order to evaluate chip area occupation. It should be considered that the proposed filter scheme gives promising results to meet low frequency applications. Also, it is considered that large numbers of advanced electrical engineering applications usually make use of infinite impulse response (IIR) filters in order to reach market's trends. Especially, some applications such as video processing, digital signal processing and high-speed digital communication necessitate computational efficiency and low latency. In this regard, the proposed architecture can be a candidate solution in the low frequency applications where reconfigurable digital IIR filters are needed. The proposed filter's cut-off frequency can be safely tunable up to 1.5MHz, whereas filter's type can be adjustable in 4th order topology such as low-pass, high-pass or Chebyshev, Butterworth configurations.

Author Contribution

Author approves sole responsibility for the parts of study: study conception and design, data collection, analysis and evaluation of the results, and manuscript preparation.

Conflict of Interest

Author declares that he has no conflicts of interest.

REFERENCES

[1] C.J. Kikkert "A Phasor Measurement Unit Algorithm Using IIR Filters for FPGA Implementation", Electronics, vol. 8, no. 12, pp. 1523-1540, 2019.

[2] F. Capligins, A. Litvinenko, D. Kolosovs, M. Terauds, M. Zeltins, and D. Pikulins "FPGA-Based Antipodal Chaotic Shift Keying Communication System", Electronics, vol. 11, no. 12, pp. 1870-1892, 2022.

[3] G. Tatar, O. Kılıç, and S. Bayar "FPGA Based Fault Distance Detection and Positioning of Underground Energy Cable by Using GSM/GPRS", In IEEE International Symposium on Advanced Electrical and Communication Technologies (ISAECT), pp. 1-6, 2019.

[4] G. Tatar, İ. Çiçek, and S. Bayar "FPGA design of a fourth order elliptic IIR band-pass filter using LabVIEW", European Journal of Science and Technology, vol. 26, no. 1, pp. 122-127, 2021.

[5] D. Datta, and H.S. Dutta, "High performance IIR filter implementation on FPGA", Journal of Electrical Systems and Information Technology, vol. 8, no. 2, pp. 1-9, 2021

[6] M.A.A. Al-Dulaimi, H.A. Wahhab, and A.A. Amer "Design and Implementation of Communication Digital FIR Filter for Audio Signals on the FPGA Platform", Journal of Communications, vol. 18, no. 2 pp. 89-96, 2023.

[7] V. Thamizharasan, and N. Kasthuri "FPGA implementation of high performance digital FIR filter design using a hybrid adder and multiplier", International Journal of Electronics, vol. 110, no. 4, pp. 587-607, 2023.

[8] S.M.R. Islam, R. Sarker, S. Saha, and A.N. Uddin "Design of a programmable digital IIR filter based on FPGA", In IEEE International Conference on Informatics, Electronics & Vision (ICIEV), pp. 716-721, 2012.

[9] H.R. Faleh "Performance investigation of digital lowpass IIR filter based on different platforms", International Journal of Electrical and Computer Engineering Systems, vol. 12, no. 2, pp. 105-111, 2021.

[10] E. Barhoumi, Y. Charabi, and S. Farhani "FPGA Application: Realization of IIR filter based Architecture", Journal of VLSI Circuits and Systems, vol. 5, no. 2, pp. 29-35, 2023.

[11] V. Vijay, V.S. Rao, K. Chaitanya, S.C. Venkateshwarlu, C.S. Pittala, and R.R. Vallabhuni "High-Performance IIR Filter Implementation Using FPGA", In IEEE 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST), pp. 354-358 2022.

[12] J. Wu, and J. Xu "Research on noise impact of building environment based on FPGA high-performance algorithm", Microprocessors and Microsystems, vol. 80, no.1, pp. 103342-103349, 2021.

[13] A. Volkova, M. Istoan, F. De Dinechin, and T. Hilaire "Towards hardware IIR filters computing just right: Direct form I case study", Computers, IEEE Transactions on, vol. 68, no. 4, pp. 597-608, 2018.

[14] R. Garcia, A. Volkova, M. Kumm, A. Goldsztejn, and J. Kühle "Hardware-aware Design of Multiplierless Second-Order IIR Filters with Minimum Adders", Signal Processing, IEEE Transactions on, vol. 70, no. 1, pp. 1673-1686, 2022.

[15] A.I. Al-Shueli "Optimized Implementation of ECG Signal Noise Cancelation Using FIR and IIR Filter Techniques Based On FPGA", Eurasian Journal of Engineering and Technology, vol. 9, no. 1, pp. 43-54, 2022.

[16] V. Pathak, S.J. Nanda, A. M. Joshi, and S.S. Sahu "FPGA implementation of high‐speed tunable IIR band pass notch filter for identification of hot‐spots in protein", International Journal of Circuit Theory and Applications, vol. 49, no. 11, pp. 3748-3765, 2021.