INTERNATIONAL SCIENTIFIC AND VOCATIONAL JOURNAL (ISVOS JOURNAL)

Vol.: 7 Issue: 2 Date: 31.12.2023 Received: 07.11.2023 Accepted: 19.12.2023 Final Version: 30.12.2023

ISVOS Journal, 2023, 7(2): 137-148 – DOI: 10.47897/bilmes.1387626

Lossless Grounded Capacitance Multiplier Based On Two CFOAs

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Abstract

A new lossless grounded capacitance multiplier (GCM) based on two current-feedback operational amplifiers (CFOAs) is proposed. The proposed circuit is built with a least number of passive elements. The capacitor is selected as grounded in the proposed circuit, while one resistor is grounded and the other is floating. The proposed GCM has low power consumption and a very large multiplying factor. The passive element matching conditions are not necessary for the designed GCM. The SPICE program is used for the simulations, and all the simulations are performed with 0.18µm CMOS technology parameters. The simulation results verify the ideal results from 10Hz to 15MHz. Further, the designed GCM is tested in the application circuit, which is a second-order passive filter. The experiments of the desgined GCM are achieved by using AD844s instead of CFOAs.

Keywords: "Grounded capacitance multiplier, CFOA, AD844, current mode, lossless."

1. Introduction

The capacitor has an important role as a passive element in analog circuits such as oscillators, analog passive and/or active filters, etc. High-valued capacitors are not preferred because they occupy large areas in integrated circuits (ICs), as referred to in [1]. That means the area of the ICs is increased if the capacitor value is increased. Thus, the capacitance multiplier circuits designed with active devices are used instead of the capacitors in ICs. Current-mode (CM) active devices have several possible advantages over voltage-mode active devices such as operational amplifiers [2-6]. The current-feedback operational amplifier (CFOA) is one of the most preferred CM active devices in CM signal processing and low-power applications [7, 8]. There are some grounded capacitance multipliers (GCMs) based on CFOAs in the literature [9-20], and some GCMs based on other active devices in the literature [21-33]. Nevertheless, GCMs in [9-33] suffer from the following disadvantages:

i) A floating capacitor is used in the circuits of [9-11, 21-27], so they need to occupy with double poly in IC technology [34]. ii) GCMs in [11-13, 23] are designed with more than one floating resistor. iii) Several GCMs in [13-16, 22, 26-28, 33] include a capacitor in series to the *X* terminal of the CFOA; therefore, they have limitations at high frequency [35]. iv) The GCM in [14, 23] is built with different types of active devices. v) The circuit in [17, 25, 28-32] can be constructed with more than two commercially active devices. vi) The GCMs described in [10-13, 17-19, 21-26, 30-32] have less operating frequency range in the scale of the decade than the proposed GCM. vii) Some GCMs are lossy [27-29].

This manuscript proposes a lossless grounded capacitance multiplier, which is based on two CFOAs. The proposed lossless GCM is designed with a least number of passive elements. The capacitor is selected as grounded in the proposed circuit, while one resistor is grounded and the other is floating. The passive element matching conditions are not necessary for the designed lossless GCM. The non-ideal and ideal analysis is also computed. In addition, the parasitic impedance effects are investigated. The simulations of the designed lossless GCM are made by the SPICE program. Further, the designed GCM is tested in the second-order passive filter. The proposed circuit is experimentally constructed with two commercially active devices.

The next sections of this manuscript are planned as follows: In the second section, the CFOA is presented, and the theoretical analyses of the designed GCM are defined. The outcomes of the simulation results are given in Section 3. The proposed lossless GCM is tested in the second-order passive filter application circuit in Section 4. In the fifth section, the outcomes of the experimental results are presented. Lastly, the conclusion is discussed in Section 6.

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Tolga Yucehan (the author) is one of the Editor-in-Chief of this journal (International Scientific and Vocational Studies Journal). The author did not serve as an Editor-in-Chief during the reviewing process of this manuscript. The editorial process of this manuscript was carried out by Umut Saray who is the other Editor-in-Chief of this journal.

2. Proposed Lossless GCM

The symbolic representation of the CFOA containing the parasitic impedances is indicated in Fig. 1. The mathematical relations of terminals of the CFOA with the parasitic impedances and the non-ideal gains can be defined in (1).

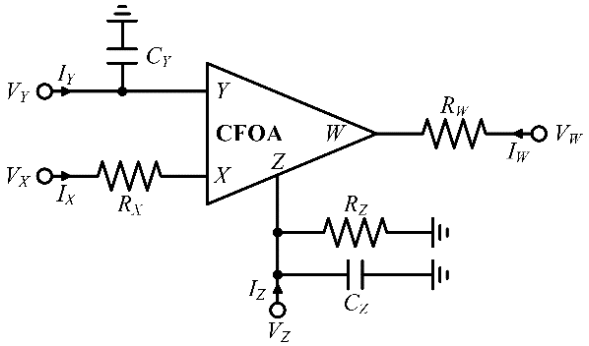

Fig. 1. Block representation of CFOA with the parasitic impedances.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} sC_Y & 0 & 0 & 0 \\ \beta & R_X & 0 & 0 \\ 0 & \alpha & sC_Z + 1/R_Z & 0 \\ 0 & 0 & \eta & R_W \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_W \end{bmatrix} \tag{1}$$

In (1), β and η are frequency-dependent non-ideal voltage gains, while α is current gain. All non-ideal gains are equal to 1, ideally. The parasitic resistor R_Z is ideally infinity, while R_X and R_W are ideally equal to zero. Also, the parasitic capacitors, named C_Y and C_Z, are ideally equal to zero. The designed lossless GCM is demonstrated in Fig. 2.

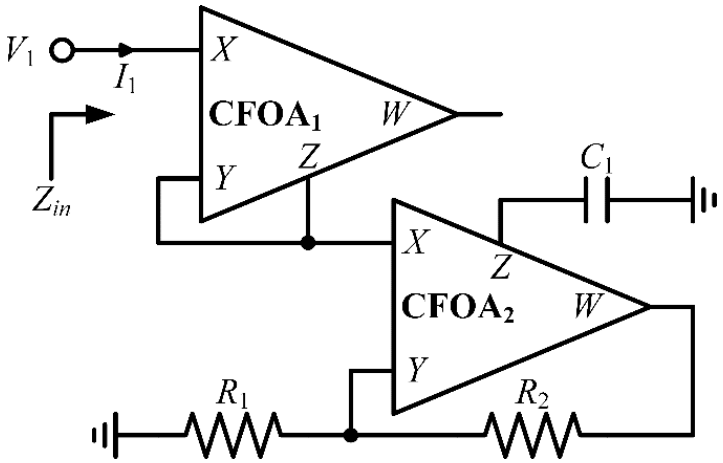

Fig. 2. The proposed lossless GCM based on CFOAs.

If the parasitic impedances of the CFOAs are comprised, and their non-ideal gains are neglected, the input impedance (Z_{in}) of the designed GCM is calculated as in (2).

$$Z_{in} = \frac{1 - R_{X1}Y_a + Y_c\left(1 + Y_b\left(R_2 + R_{W2}\right)\right)\left(R_{X1} - R_{X2} + R_{X1}R_{X2}Y_a\right)}{Y_c\left(1 + Y_b\left(R_2 + R_{W2}\right)\right)\left(1 + R_{X2}Y_a\right) - Y_a} \tag{2}$$

Here, $Y_a = sC_{Y1} + sC_{Z1} + 1/R_{Z1}$, $Y_b = sC_{Y2} + 1/R_1$, and $Y_c = sC_1 + sC_{Z2} + 1/R_{Z2}$. If β, η, and α of the CFOAs are included, and their parasitic impedances are neglected, Z_{in} is computed as in (3).

$$Z_{in} = \frac{\alpha_1\alpha_2\beta_1\beta_2\eta_2}{sC_1\left(1 + R_2 / R_1\right)} \tag{3}$$

If β, η, and α and the parasitic impedances of the CFOAs are neglected, Z_{in} is defined as in (4).

$$Z_{in} = \frac{1}{sC_1\left(1+R_2/R_1\right)} = \frac{1}{sC_1K} = \frac{1}{sC_{eq}} \tag{4}$$

Here, K is the multiplying factor, which is equal to $1+R_2/R_1$, and the equivalent capacitance (C_{eq}) of the designed GCM is equal to $C_1\times(1+R_2/R_1)$.

3. Simulation Results of The Proposed GCM

The internal structure of the CFOA based on the MOS transistor is given in Fig. 3 and derived from [36]. The equations of the small signal input and output resistances of the Fig. 3 are calculated as in (5).

$$r_X = \frac{r_{O5}}{\left(\frac{1}{g_{m4}}+\frac{1}{g_{m12}}\right)\left(r_{O1}//r_{O21}\right)\left(r_{O17}//r_{O25}\right)g_{m17}g_{m19}g_{m21}} \tag{5a}$$

$$r_Z = \left(r_{O6}r_{O14}g_{m14}\right)//\left(r_{O31}r_{O36}g_{m31}\right) \tag{5b}$$

$$r_W = \frac{r_{O13}}{\left(\frac{1}{g_{m10}}+\frac{1}{g_{m15}}\right)\left(r_{O7}//r_{O23}\right)\left(r_{O18}//r_{O27}\right)g_{m18}g_{m20}g_{m23}} \tag{5c}$$

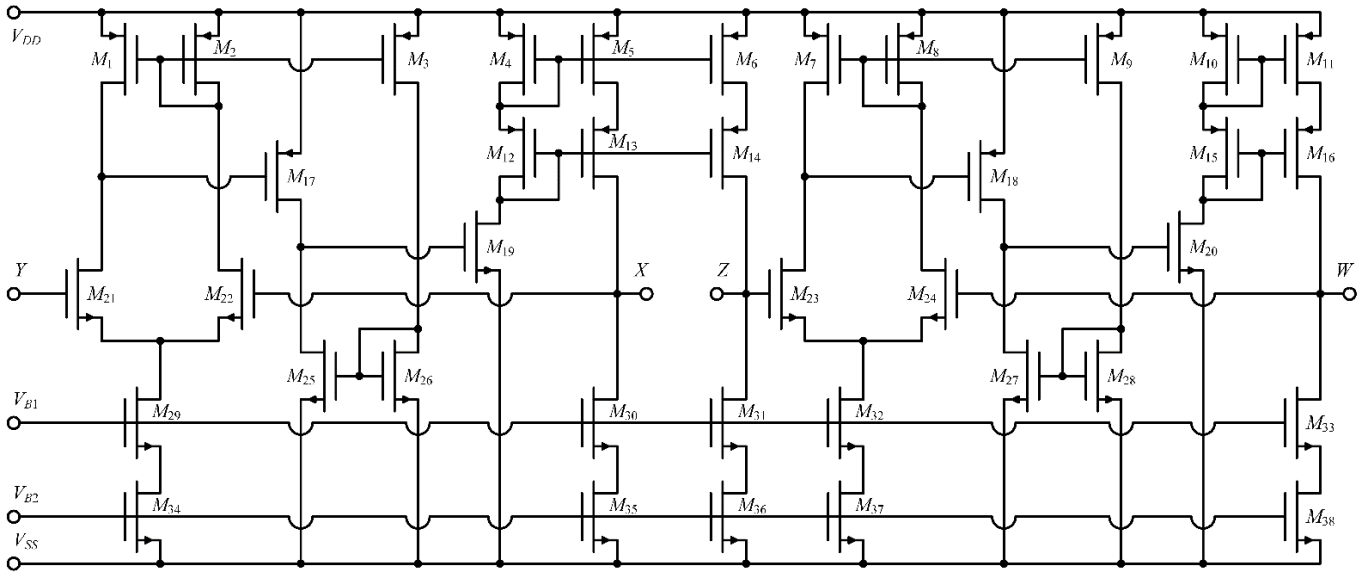

Fig. 3. The internal structure of the CFOA derived from [36].

The width (W) and length (L) parameter values of the MOS transistors of the CFOA are shown in Table 1. The simulations are made with 0.18µm CMOS technology parameters [37] for the MOS transistors in Fig. 3. The bias voltages are taken as $V_{B1} = -0.02$ V and $V_{B2} = -0.45$ V, and the supply voltages of the internal structure are selected as ±0.9 V. As a result of selecting these values, the β, η, and α and the parasitic impedances of the CFOA are computed as in Table 2.

Table 1. The width and length parameter values of the MOS transistors.

Transistors		L (µm)	W (µm)
PMOS	M_1-M_{18}	0.5	4
NMOS	M_{19}-M_{28}, M_{30}, M_{31}, M_{33}, M_{35}, M_{36}, M_{38}	0.5	2
	M_{29}, M_{32}, M_{34}, M_{37}	0.5	12

Table 2. Values of the some performance parameters of the CFOA.

Parasitic Impedances of The CFOA					
$R_X \cong 27.8\Omega$	$R_Z \cong 0.378G\Omega$	$R_W \cong 27.8\Omega$	$C_Z \cong 6.2fF$	$C_Y \cong 1.8fF$	
Non-ideal Gains of The CFOA					
$\alpha = 1.0000$	$\beta = 1.0000$	$\eta = 1.0000$	$f_\alpha \cong 140MHz$	$f_\beta \cong 147MHz$	$f_\eta \cong 191MHz$

The SPICE program is used to make all simulations. R_1 and R_2 resistors of the proposed GCM are chosen as 1k**Ω** and 9k**Ω**, respectively. Also, the capacitor C_1 in Fig. 2 is selected as 100pF. As a result, K and C_{eq} are ideally found as 10 and 1nF, respectively. In Fig. 4, the outcomes of the AC analysis results for the designed lossless GCM are shown comparatively with the ideal results. The Monte Carlo (MC) analysis outcomes are given in Fig. 5, in which Gauss deviations of all the passive elements are taken as 5 %. The MC analysis is made with 200 samples. In Fig. 6, the AC temperature analysis outcomes are demonstrated where the temperature is varied from -60ºC to 120ºC, with the Gauss deviation chosen as 5 %. In the temperature analysis, the linear temperature changes of all the resistors for 1ºC are taken as 15 ppm. In addition, the time-domain analysis is performed for the proposed GCM, and the results are indicated in Fig. 7. An input current that has 0.5µA magnitude at 100kHz is applied to the proposed GCM for the time-domain analysis. Fig. 8 shows the magnitude and phase results comparatively with the ideal results for different K values. In this simulation, resistor R_1 is selected as 1k**Ω**, while R_2 is chosen as 9k**Ω**, 99k**Ω**, and 999k**Ω**, respectively. Capacitor C_1 is selected the same as with other simulations. Consequently, K is calculated as 10, 100, and 1000, while C_{eq} is 1nF, 10nF, and 100nF. The total power consumption of the designed lossless GCM is about 62.9µW.

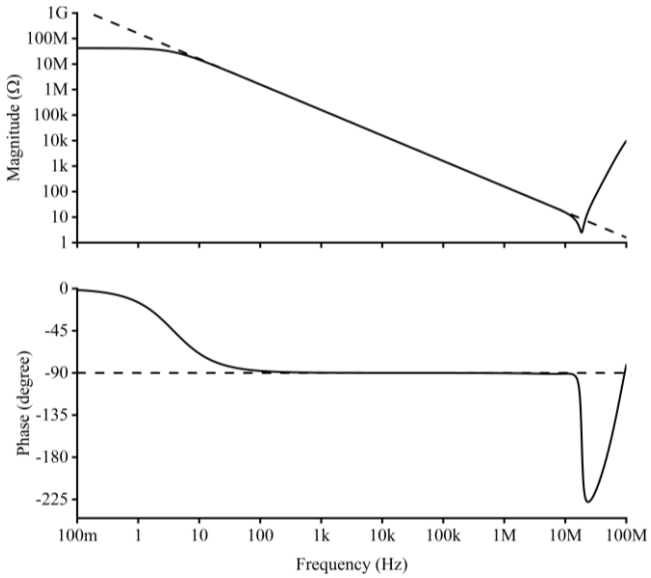

Fig. 4. AC impedance results of the designed GCM.

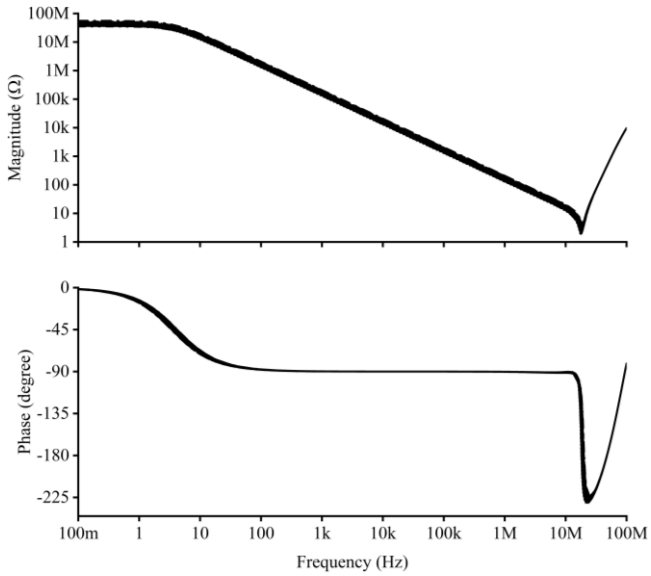

Fig. 5. Outcomes of the MC analysis results for the proposed designed GCM.

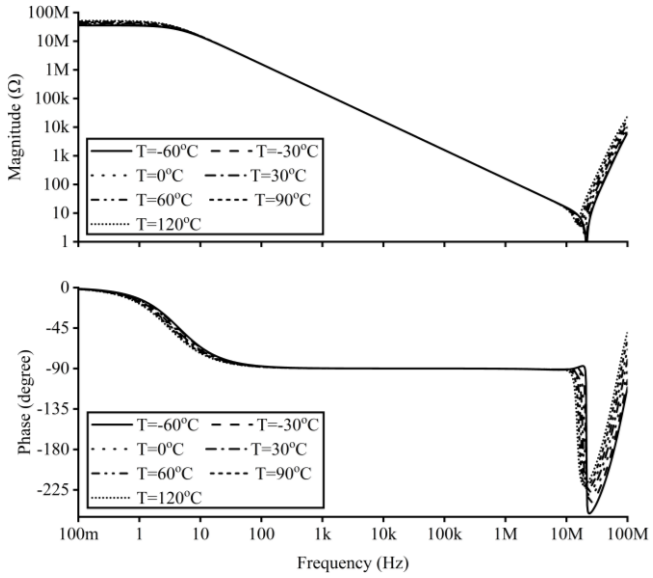

Fig. 6. Temperature analysis results of the designed lossless GCM.

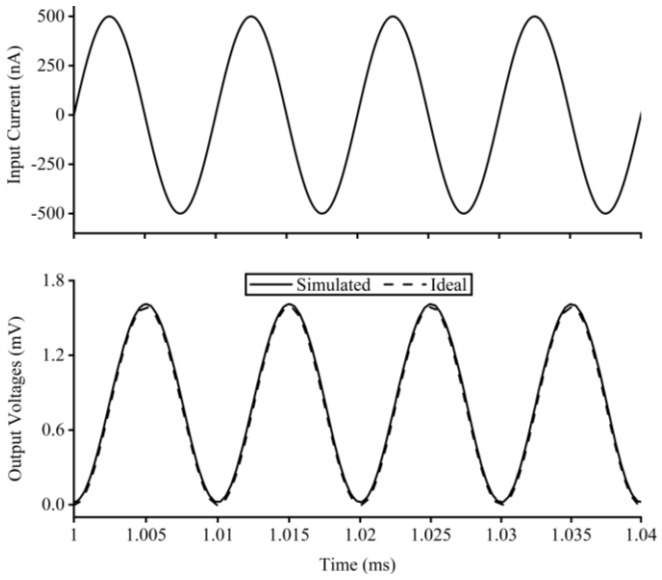

Fig. 7. The input current and output voltages of the designed lossless GCM.

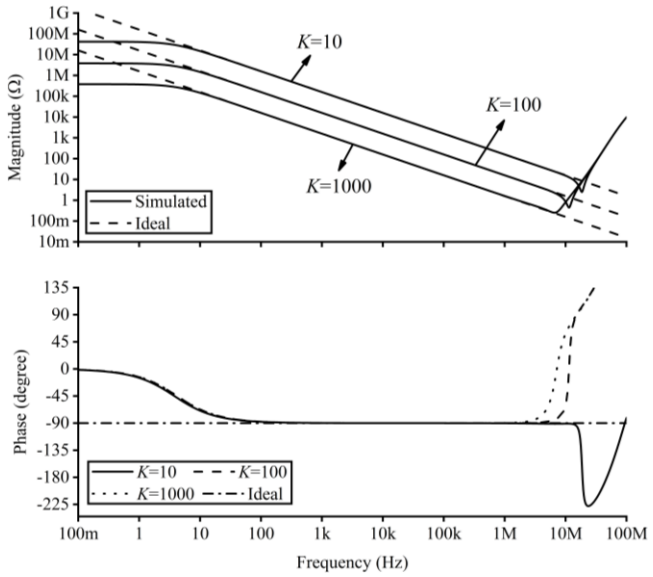

Fig. 8. AC impedance results of the designed lossless GCM for different multiplying factors.

The comparison table for the proposed GCM with the CFOA-based GCMs in [9-20] is shown in Table 3. In Table 3, Figure of Merit (FoM) is a term that is related to operating frequency range, supply voltages, total power consumption, and number of active devices. Also, FoM is shown in (6) as an equation. According to Table 3, if the power consumption, operating frequency range, K, and supply voltages are considered together, the proposed circuit is assumed to be more advantageous than other circuits in Table 3.

$$\text{FoM}=\frac{\text{Operating Frequency Range}}{\text{Supply Voltages}\times\text{Total Power Consumption}\times\text{Number of Active Devices}} \tag{6}$$

Table 3. The comparison table for the CFOA-based GCMs in [9-20] with the proposed GCM.

References	Figure	# of Active Devices	# of *C* / *R*	# of Floating Capacitor	# of Floating Resistor(s)	Technology	Supply Voltages (V)	Power Dissipation (mW)	Operating Frequency Range (Hz)	Operating Frequency Range (decade)	*K*	FoM
[9]	2c	2 CFOA	1 / 2	1	0	–	–	–	–	–	50	–
[10]	2	2 CFOA	1 / 2	1	1	0.35µ	±0.75	0.507	5.75 – 512.8k	4.95	5	117.27M
[11]	4	1 CFOA	1 / 2	1	2	AD844	–	–	1k – 1M	3	10	–
[12]	3	2 CFOA	1 / 2	0	2	AD844	±9	233	~30 – ~30M	6	20	238.44k
[13]	2	1 ICFOA	1 / 2	0	2	0.13µ	±0.75	0.1	100k - 6M	1.78	51	800k
[14]	1	1 CFOA, 1 OTA	1 / 1	0	0	AD844, LM13700N	±5	–	2 – 7M	6.54	400	–
[15]	2	2 CFOA	1 / 2	0	1	AD844	–	–	–	–	–	–
[16]	2c	2 CFOA	1 / 2	0	1	AD844	–	–	–	–	–	–
[17]	3a	1 MCFOA	1 / 2	0	0	0.25µ	±1.5	0.52	~30k – ~30M	3	–	–
[17]	3b	1 MCFOA	1 / 2	0	0	0.25µ	±1.5	0.52	~30k – ~30M	3	–	–
[18]	2	1 ICFOA	1 / 2	0	1	0.18µ	±1.25	0.024	1 – 30k	4.48	10000	1G
[19]	3	2 CFOA	1 / 2	0	1	0.13µ	±0.75	–	100k – 100M	3	100	–
[19]	6	3 CFOA	1 / 3	0	1	0.13µ	±0.75	–	100 – 100M	6	100	–
[20]	2b	2 CFOA	1 / 2	0	1	AD844	–	–	–	–	–	–
Proposed GCM	**2**	**2 CFOA**	**1 / 2**	**0**	**1**	**0.18µ**	**±0.9**	**0.0629**	**10 – 15M**	**6.18**	**1000**	**13.25G**

–: Not available. FoM: Figure of Merit is given in (6)
MCFOA: Modified CFOA. ICFOA: Inverting CFOA. OTA: Operational transconductance amplifier.

The AC analysis performances of the GCMs in [15, 20] are compared to the proposed GCM. This comparison is made when *K* is selected as 10, and the value of the capacitor is equal to 100pF for the proposed GCM and the GCMs in [15, 20]. A comparison of AC analysis results of the GCMs in [15, 20] with the proposed lossless GCM is given in Fig. 9.

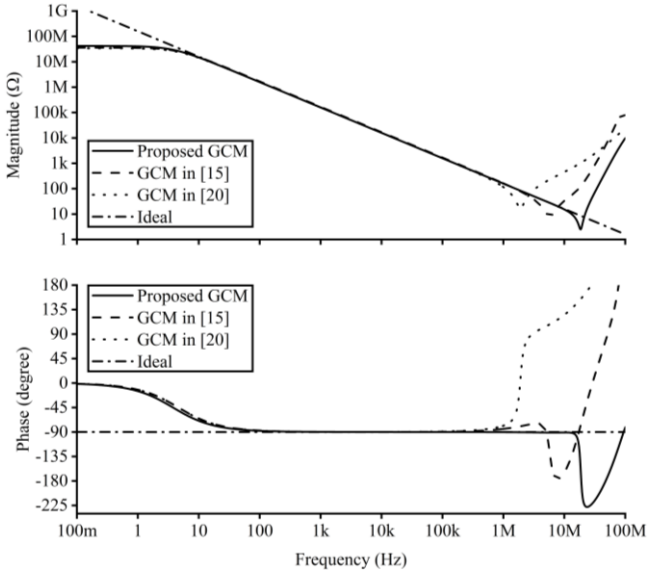

Fig. 9. A comparison of AC impedance results of the designed lossless GCM with the GCMs in [15, 20].

4. Application Example

The proposed lossless GCM is tested in the application circuit, which is a second-order passive filter shown in Fig. 10. This application circuit has two outputs. This second-order passive filter behaves as a low-pass filter (LPF) from one output and behaves as a notch filter (NF) from another output. The transfer functions (TFs) of the filter are given in (7), and (8). Also, the resonance frequency (f_0) and the quality factor (Q) are shown in (9).

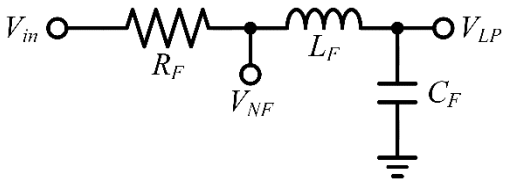

Fig. 10. Second-order passive filter.

$$TF_{LP} = \frac{1/L_F C_F}{s^2 + s\left(R_F/L_F\right) + 1/L_F C_F} \tag{7}$$

$$TF_{NF} = \frac{s^2 + 1/L_F C_F}{s^2 + s\left(R_F/L_F\right) + 1/L_F C_F} \tag{8}$$

$$f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{L_F C_F}} \tag{9a}$$

$$Q = \frac{1}{R_F}\sqrt{\frac{L_F}{C_F}} \tag{9b}$$

A resistor and an inductor in Fig. 10 are chosen as 1k**Ω** and 5mH, respectively. The proposed GCM is used instead of the capacitor (C_F) in the second-order passive filter. R_1, R_2, and C_1 of the designed lossless GCM in Fig. 2 are selected as 1k**Ω**, 49k**Ω**, and 100pF, respectively. Thus, K = 50, and C_{eq} = 5nF. Consequently, selecting these values of the application example and the proposed GCM, f_0 and Q are calculated as 31.831kHz and 1, ideally. AC frequency analysis outcomes of the filter are demonstrated in Fig. 11, while noise analysis outcomes for the LP output are represented in Fig. 12. The transient analysis is also made for the application circuit, and its results for the LP output are plotted in Fig. 13. The sinusoidal input voltage, which has 0.5mV amplitude at 1kHz, is implemented to the filter.

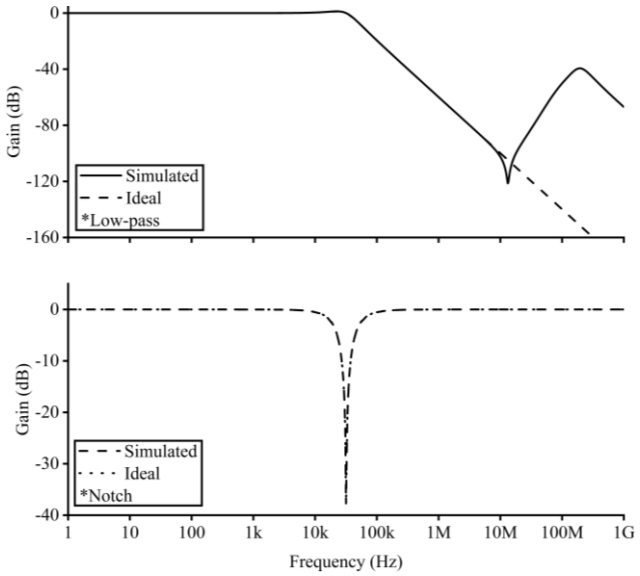

Fig. 11. The outcomes of the AC analysis results of the application example.

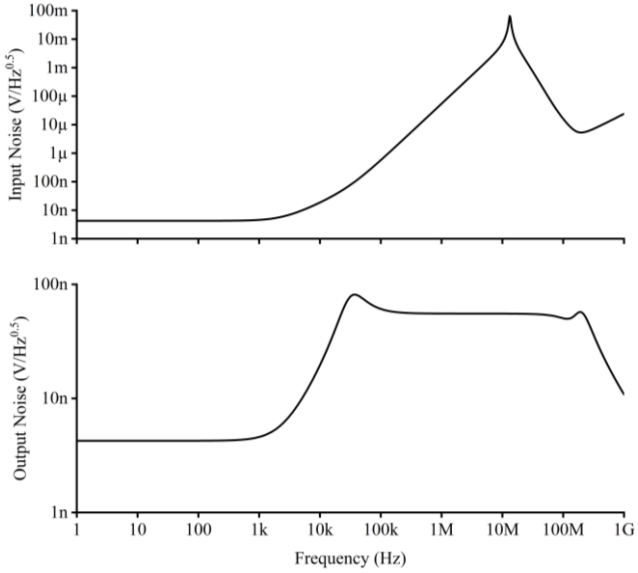

Fig. 12. The outcomes of the noise analysis results for the LP output of the application example.

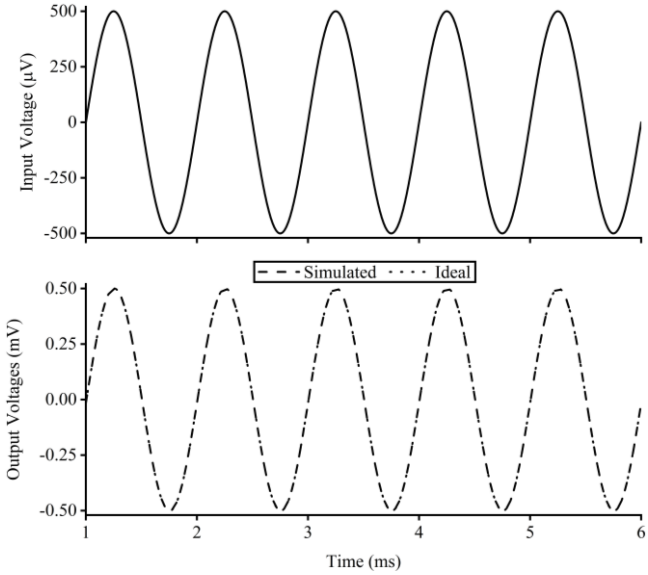

Fig. 13. The outcomes of the transient analysis results for the LP output of the application example.

5. Experiment Results

The designed GCM is implemented with AD844s [38], which are used instead of the CFOAs. AD844 is a commercially active device of the CFOA; thus, one CFOA can be built with one AD844. In Fig. 14, the experimental circuit is shown, where an additional AD844 and one resistor (R_i) are used as a current generator. The supply voltages of the AD844s are ±12V. The resistors R_1 and R_2 are taken as 1kΩ and 10kΩ, respectively, while C_1 = 1nF. As a result of selecting these values of the proposed GCM in experiments, K and C_{eq} are ideally found as 11 and 11nF. Also, R_i of the current generator in Fig. 14 is selected as 4.7kΩ. Besides, $Z_{eq} = V_{out} \times R_i / V_{in}$ is taken for the experiments. The AC magnitude and phase outcomes are given in Fig. 15. The transient analysis is also made in which a sinusoidal input voltage with 0.6V peak-to-peak magnitude at 1kHz is applied. The results of the time-domain analysis are shown in Fig. 16. As seen in Fig. 16, it is clear that there is a phase difference of approximately 90° between the input and output signals of the proposed circuit, and the input impedance of the proposed GCM has a phase of -90°.

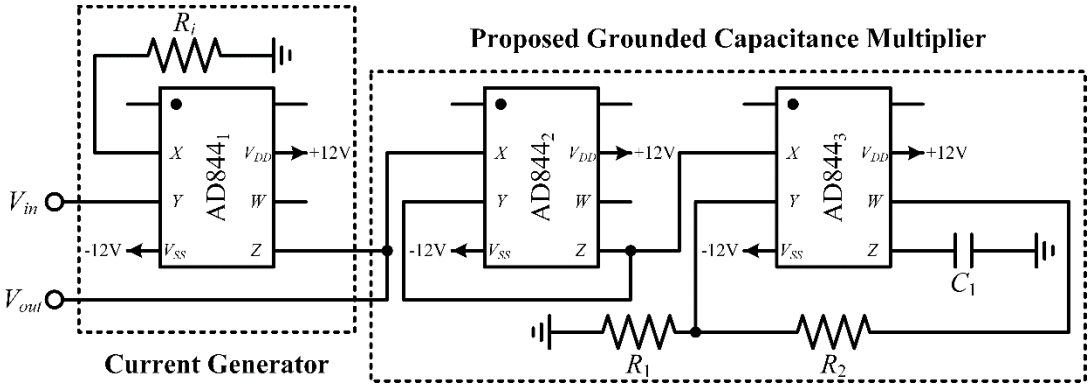

Fig. 14. Experimental circuit scheme of the proposed GCM.

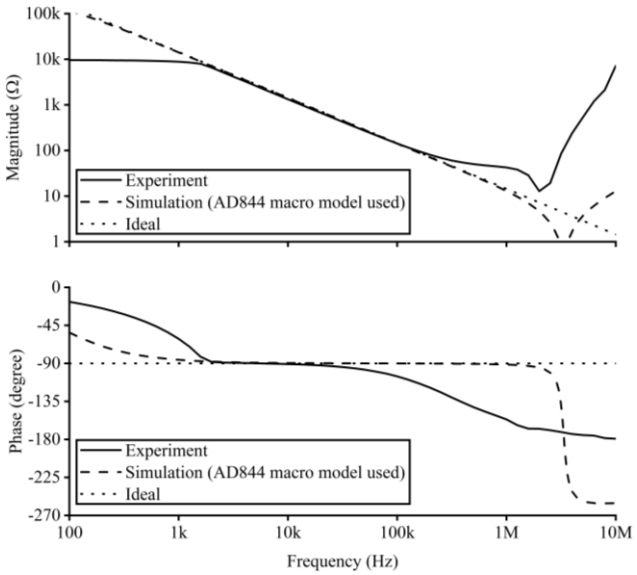

Fig. 15. The outcomes of the AC analysis results of the proposed GCM.

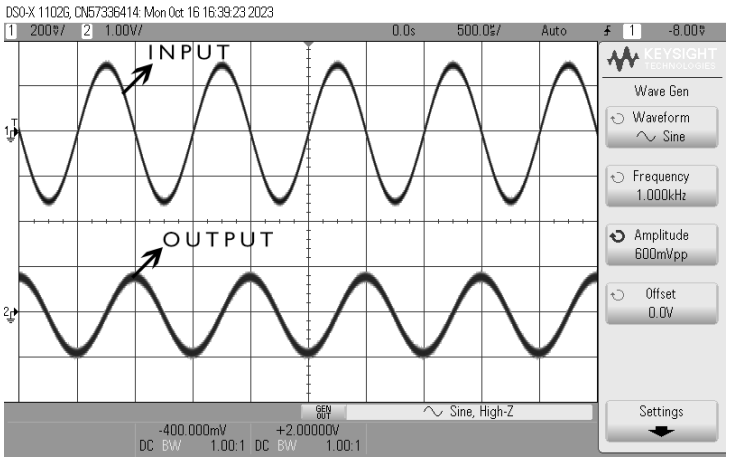

Fig. 16. Time-domain analysis outcomes of the proposed GCM.

6. Conclusion

In this manuscript, a new CFOA-based lossless GCM is designed. Two resistors, two CFOAs, and a capacitor are used in the designed GCM. The passive element matching conditions are not necessary for the designed circuit. One of the resistors is floating, and the other is grounded while the capacitor is grounded. The multiplying factor can be chosen to be very large, and the total power consumption is low enough. Simulations are performed by using the SPICE program, and the designed GCM is examined in a second-order passive filter application circuit. Also, all the simulations are performed with 0.18μm CMOS

technology parameters. The designed lossless GCM can be operated from 10Hz to 15MHz. The experiments are built on the breadboard, in which AD844s are utilized instead of the CFOAs. Also, the Keitley DSOX1102G digital oscilloscope and the Keitley 2220-30-1 DC power supply are used in the experiments. However, simulation and experiments verify the theory well, whereas parasitic impedances and non-idealities of the CFOA, parasitic impedances of the breadboard, and the non-idealities of the AD844s a bit influence the performances of the designed lossless circuit.

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