



A COMPACT GAN POWER AMPLIFIER MODULE FOR NEW GENERATION CELLULAR BASESTATIONS

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Abstract: This paper presents a compact class-AB Power Amplifier Module (PAM) designed for new generation massive Multiple Input Multiple Output (MiMo) cellular base stations. The module is designed at the center frequency of 3.5GHz targeting Long Term Evolution (LTE) and 5G New Radio (NR) bands. The module is a hybrid design that incorporates a Gallium Nitride (GaN) High Mobility-Electron Transistor (HEMT) die, discrete components-based input, and output matching networks. The entire design is realized on an 8.5 x 5.2 mm, 2-layer Rogers4003C substrate. The module is assembled on a PCB as an open-top for post-characterization tuning. The small signal and large signal measurements are in quite good agreement. The measurement results show that the amplifier is unconditionally stable, the input return loss is 12.2 dB, the output return loss is 7.7 dB, and the small signal gain is 13.4 dB. The saturated output power is 33.3 dBm with a Power Added Efficiency of 20.1%. The small signal gain drops to 11.2 dB at around 22 dBm of input power due to GaN technology's intrinsic soft compression characteristics.

Keywords: Power amplifier module, Gallium nitride HEMT, 5G n78, LTE band 42

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Received: March 19, 2024

Accepted: May 10, 2024

Published: May 15, 2024

Cite as: Türk BB, Hürçan F, Savcı HŞ, Doğan H. 2024. A compact GaN power amplifier module for new generation cellular basestations. *BSJ Eng Sci*, 7(3): 587-593.

1. Introduction

The new generation of mobile services requires several different bands both at sub-6GHz and millimeter wave frequencies. Some of them are re-allocations of intrinsic cellular bands while others are newly assigned. These new frequency bands are there to handle more data traffic with complex modulations resulting in more demanding system requirements. Such high demands from the system increased the number of base stations with higher performance but smaller coverage in a typical cell. Small-cell base stations such as Microcells, Picocells, and Femtocells, therefore, gained attraction over macro cells as they are smaller in size, emit less power, are easier on thermal control, and are more environmentally friendly (Hsu et al., 2017). The sub-6 GHz bands are expected to operate with higher consumer demand than mm-wave ones (Li et al., 2018). Regardless of the frequency band, power amplifiers are one of the key RF elements in the entire cellular transceiver design. As the generation of cellular system increase, the requirements of micro or macro base-station power amplifiers evolve to be more stringent. The transmitter of microcells, picocells, and femtocells are compact for frequent placement in indoor or outdoor locations. As part of a small transmitter, the PAs need to be designed

more compact and more power efficient in order to have a thermally stable operation. GaN devices have a higher energy gap than GaAs devices which enable them to have higher breakdown voltage and power density (Colantonio et al., 2009). The higher breakdown also allows large voltage swings and high power output. With the high output power handling capability, GaN PAs are commonly used in small cell applications. In this work, a class-AB GaN HEMT PAM is designed for new-generation cellular networks. This paper is organized as follows: The design procedure is explained in section 2 whereas the implementation and measurements are detailed in section 3 followed by a conclusion.

2. Material and Methods

The purpose of any amplifier is to produce an output that follows the characteristics of the input signal but with higher voltage or power. One of the most important blocks of wireless communication systems is RF power amplifiers. RF Power amplifier design entails multiple design challenges such as linearity, gain, stability, output power, input and output matching, and thermal (Ozalas, 2021). The topology and transistor selection play a critical role in overcoming all these challenges. The PAM is realized on a 8.5x5.2mm sized 20-mil thick Rogers



4350C low-loss RF substrate with 1oz copper on both sides. A 8W GaN HEMT transistor (Cree’s CGH60008D) and 0603 sized discrete components are used. GaN technology is chosen for its higher breakdown voltage, larger power density, and broader bandwidth. The PAM is designed in Class AB mode operation to optimize between Power Added Efficiency (PAE) and linearity (Monprasert et al., 2010). The quiescent operating drain current I_{ds} is 134 mA for the drain voltage V_{ds} of 28 V, which corresponds to the gate voltage $V_{gs} = -2.7$ V where the performance optimization for the desired linearity at the highest efficiency is obtained (Iqbal and Piacibello, 2016). The HEMT die is attached to the laminate using the 25 μ m gold bond wires for the gate and the drain connections. The effects of wirebonds were included in the design process with the proper EM-based model where the mutual inductance and capacitance among multiple wires and the ground plane is included (Nazarian et al., 2012). Figure 1 shows the simplified schematic of the proposed PAM.

The design is optimized through the simulations using vendor-supplied component models and EM simulations of laminate layout and bond wires. The HEMT device model includes large signal behavior which enables harmonic balance simulations. Therefore, besides small-signal characterization, the load pull simulations were done to optimize the output matching network based on the AM-to-AM and AM-to-PM nonlinearities of the transistor. The output matching network is designed using iterative load-pull and source-pull simulations to ensure optimum performance of the PAE and the 3rd order output Intercept Point (OIP3) for targeted power delivery (Tao et al., 2015). The source and load impedances for the maximum gain, the optimum OIP3 and the PAE for the transistor were $3.2-j*7.7 \Omega$ and $24.5+j*12.9 \Omega$ respectively at the center frequency between the 3.4 GHz and 3.6 GHz frequency bands. The

input and output matching circuits were realized with lumped elements. The input matching network was designed with a high-pass T-type topology where the effects of gate bias and stability networks are embedded in the matching. The output network is designed with a DC-blocked low-pass L topology where the supply network is used for 2nd harmonic optimization. The supply decoupling capacitors were also added at both the gate and the drain bias lines. The proper stability network consists of a shunt series RC network at the input of the PAM. The design is optimized using parametric schematic and EM simulations. The topology and final component values are given in Figure 1.

Figure 2 shows the simulated performance. The saturated output power is 37.1 dBm for an input power of 24.75 dBm which corresponds to 12.35 dB gain 39% and power-added efficiency at about 1dB compression point. A 100 Ω resistor was used as the stability network. Figure 3 shows the result of a parametric study of the stability resistor over the input and the output return loss. Small signal stability analysis is a common method used in the design of RF amplifiers. In an amplifier, the closed loop gain of a classical feedback system shown in Equation (1) should satisfy the stability condition for each feedback loop including the ones caused by the parasitic electric and magnetic couplings. Here, A presents the open loop gain of the amplifier, and β presents the feedback network transfer function. If the $A\beta$ which is the loop gain, has the amplitude of 1 with the phase of π the amplifier becomes unstable (Sedra et al., 2021).

This approach has been widely used in the design of power amplifiers to analyze the stability (Zhao et al., 2022). Besides many parasitic feedback loops, the parasitic effects coming from the finite impedance ground connection at the source of the active device can be considered the strongest feedback path in the system.

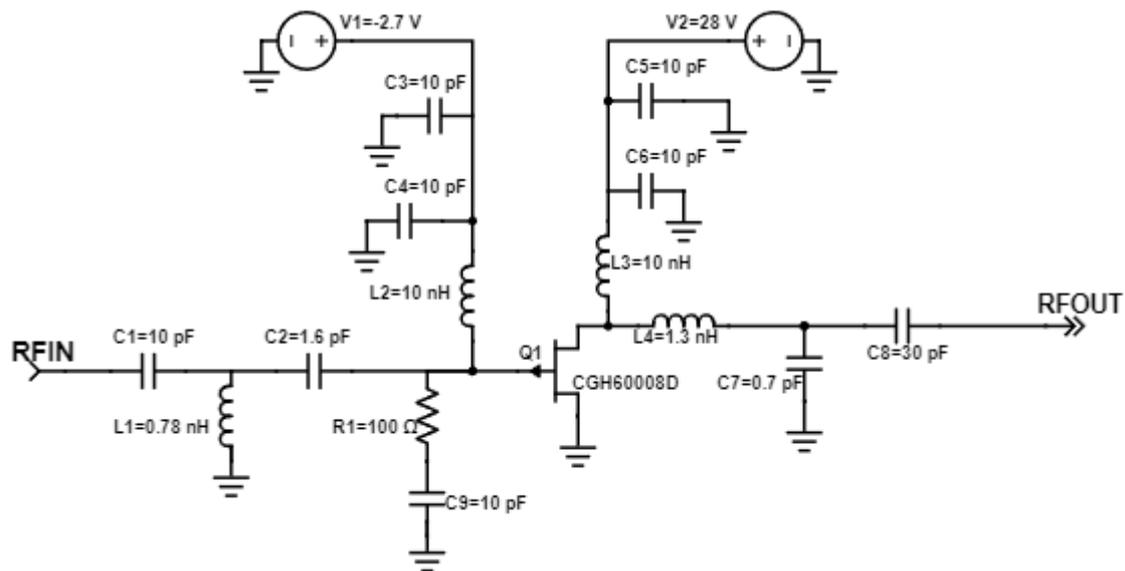


Figure 1. Schematic of proposed module design.

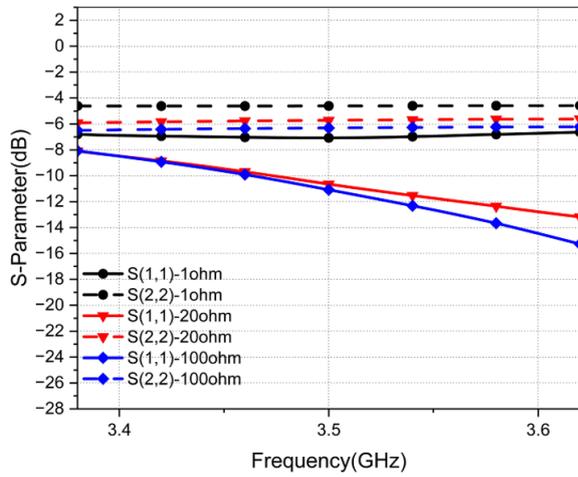


Figure 3. Parametric study of stability resistor values.

$$A_f = \frac{A}{1 + A\beta} \tag{1}$$

The stability condition was simulated for the input power of 24.75 dBm which corresponds to 5W output power. Figure 5 shows the loop gain from DC to 10 GHz at the drain and the gate nodes. It is observed that the circuit is stable as the loop gains for both cases are below -15 dB. Although small signal stability is a commonly checked one, power amplifiers are typically used under large signal conditions. In addition to small signal stability analysis, the stability conditions under large signal presence should also be checked. In this work, the large signal stability analysis was done and a test setup was constructed to simulate the large signal conditions. In addition to the loop-gain-based stability criteria, another method, which is based on the driving point impedance technique, was used to check stability (Bode, 1945). The driving point impedance is the network determinant divided by the same determinant with the node that is selected, discarded from the network matrix. Same condition can be considered for the admittance. Figure 4 shows the network built with admittance nodes.

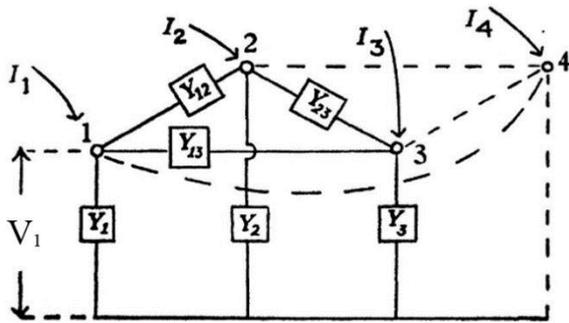


Figure 4. Admittance network.

Considering the current flow and node voltages driving point admittance can be calculated. Y-matrix is built with a set of nodal equations. The nodal equation in Equation (2) is an example of current equation at node 1 where \$Y_{11}\$ can be written as Equation (3). Just like \$Y_{11}, Y_{22}\$ or any \$Y_{nn}\$ can be written in this form. Thereon, Equation (4) is

created with the admittance of the nodes. Discarding the node from the matrix means the column and row which contains the node is removed from the matrix. This means that in Equation (4), the determinant of the matrix with the removal of node 2, discards \$Y_{22}\$ along with the \$Y_{21}\$ and \$Y_{12}\$ from the matrix and only \$Y_{11}\$ remains. Normally the matrix determinant of the admittance network is \$Y_{11}Y_{22} - Y_{21}Y_{12}\$; however, removal of the node 2 divides the determinant with the remaining \$Y_{11}\$ and driving point admittance of node 2 becomes Equation (5).

$$Y_{11}V_1 - Y_{12}V_2 - \dots - Y_{1n}V_n = I_1 \tag{2}$$

$$Y_{11} = Y_1 + Y_{12} + \dots + Y_{1n} \tag{3}$$

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{4}$$

$$\frac{\Delta'}{\Delta'_{22}} = \frac{Y_{11}Y_{22} - Y_{21}Y_{12}}{Y_{11}} \tag{5}$$

In other words, the driving point admittance of a node is the ratio between the driving current entering the node and the node voltage that results in. If the node self-oscillates, the response of the network may give unexpected results (Ozalas, 2021). Moreover, Kurokawa (1969) also checks the stability with the impedance response. If the real part of the impedance is either zero or negative, while the slope of the imaginary part increases with the frequency increase, the self-oscillation condition occurs. Figure 6 points out the real value of driving point admittance for the gate and drain nodes of PAM from DC to 10 GHz. It is observed that the minimum value is 0.011 which concludes that the PAM is stable for the entire frequency range. Kurokawa condition was also checked with driving point admittance. Since the sign of the impedance is crucial for Kurokawa condition driving point admittance result can be used. It assured the PAM's unconditional stability as well.

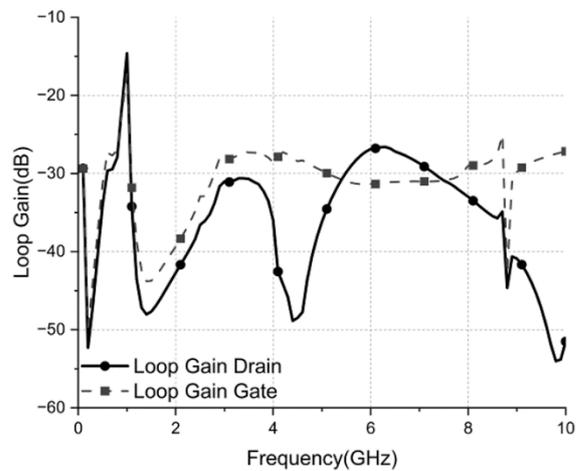


Figure 5. Logarithmic loop gain of PA.

An evaluation board was designed as a connectorized testing vehicle for small signal and large signal measurements of the PAM. The Figure 7 shows the die

picture and the evaluation board. The board includes 2 input and output SMA connectors, 2 DC bias pins, and 2 extra pins for merging the ground connections of the

supplies. A finned aluminum plate is attached to the back of the board for proper heat dissipation. The size of the evaluation board is 26 x 21 mm².

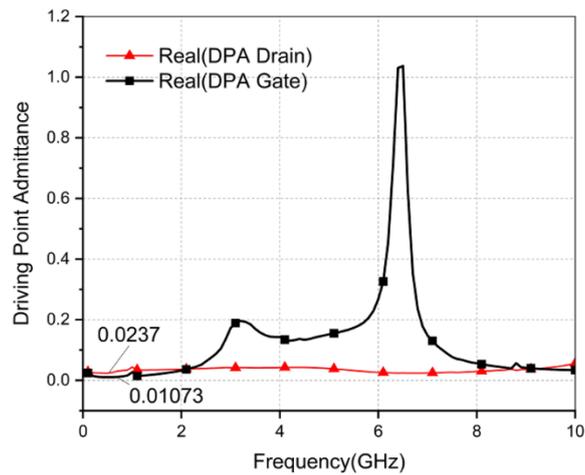


Figure 6. Driving point admittance of PA.

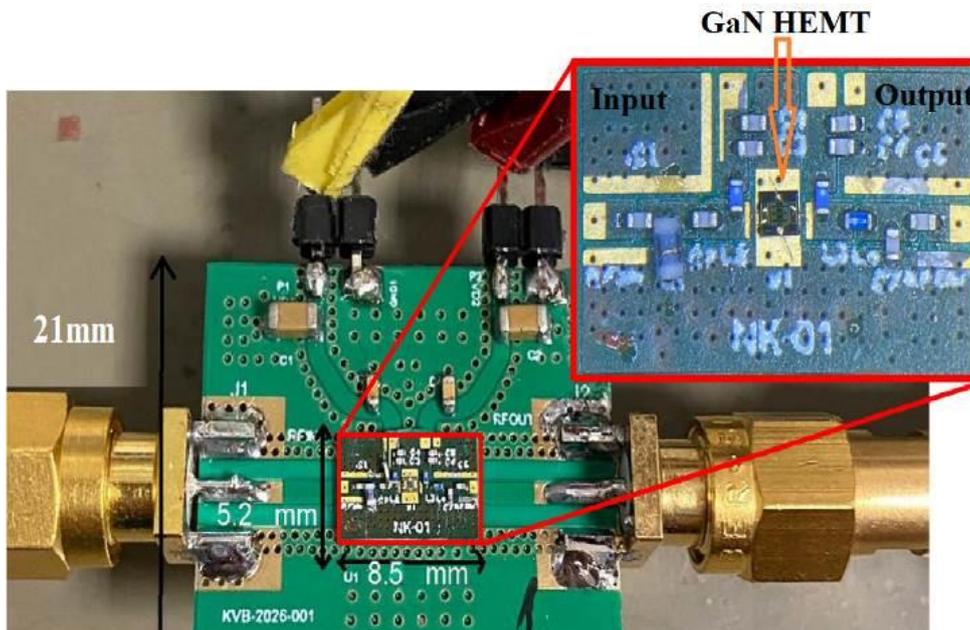


Figure 7. The assembled power amplifier module.

3. Results and Discussion

The laminate is manufactured with solder mask and silkscreen. Die placement, component assembly and wire bondings are manually done. The GaN HEMT die has gold back plate. Therefore, electrically conductive Epotek H20e silver epoxy was used for die bonding. 25 μ m gold wirebonds are for gate and drain connections. Although there is thru-wafer-via in the GaN die extra downbonds are added for RF grounding. The board was characterized for both small signal and large signal performance at Istanbul Medipol University RF Laboratory.

3.1. Small Signal Measurements

The small signal response of the PAM was measured by Rohde&Schwarz ZNB8 model Vector Network Analyzer. Figure 8 shows the simulation and measurement results for small signal gain, input return loss and output return loss. At 3.5 GHz the gain was measured as 13.4 dB, the

output return loss was measured as -7.7 dB and the input return loss was measured as -12.2 dB. The small signal stability indicators of μ and μ' values were calculated from the measured S-parameters (Colantonio et al., 2009). As both the μ and μ' are greater than 1 across a broad frequency range, the PAM was unconditionally stable under small-signal conditions.

3.2. Large Signal Measurements

The large signal response of the PAM was tested with a 3.4 GHz single tone supplied by the Rohde&Schwarz SMB100A signal generator and a Mini Circuits ZHL-5W-63-S+ driver amplifier, and the output of PAM was monitored with the Rohde&Schwarz FSH8 spectrum analyzer. The block diagram of the test setup is shown in Figure 9. A 30 dB attenuator was used for protection of the spectrum analyzer from the incidence of high-power signal. Likewise, two 10 dB attenuators in the setup were

used for protection of DUT, preamplifier and the signal generator from the incidence or reflectance of high-power signals under high VSWR conditions (Mini-Circuits, 2020). To measure the large signal response of PAM, the signal generator was swept in the range of -30 dBm to -8 dBm, so that the preamplifier can drive the DUT with signal levels between 0 dBm to 22 dBm. The measurements were performed in short periods and with a running cooler fan in order to thermally stress the PAM. The output power and supply currents were recorded for each input power value and post-measurement calculations were done.

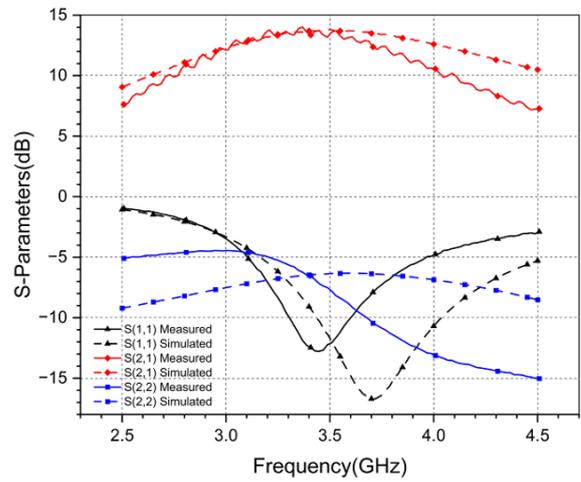


Figure 8. S-parameter vs frequency for measurement and simulation.

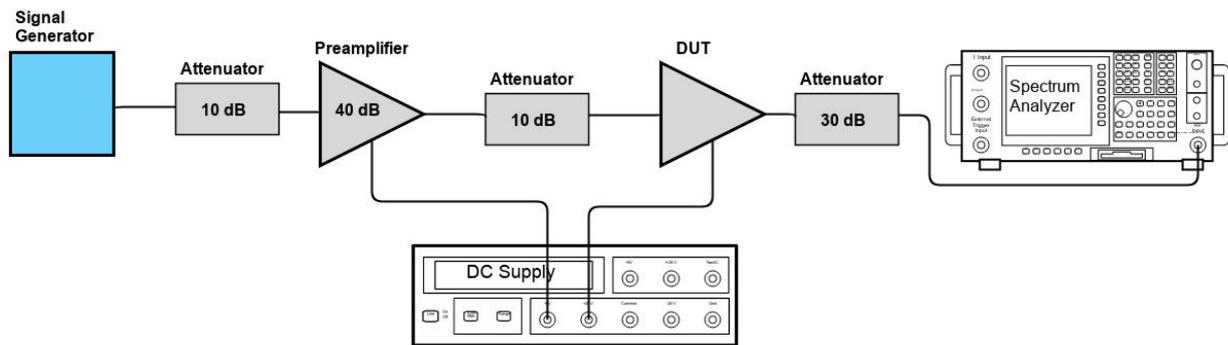


Figure 9. The block diagram of the proposed large signal test.

Figure 10 shows the output power and transducer power gain at 3.4 GHz. The cable losses and test setup losses were de-embedded from the large signal measurements. The measurement was done only up to the output of 33.2 dBm due to the driving power limitations in our measurement setup. The maximum output power was measured as 33.3 dBm without any compression. The gain was flat for the input power range from 17 to 22 dBm. The transducer power gain is greatly affected by the mismatches at both input and output. Figure 10. Measurement of output power, gain at 3.4 GHz. Table 1 shows the comparison of similar hybrid power amplifier module studies in the literature. The measured PAE was only reported up to a power output of 33.2dBm due to the driving power limitations in our measurement setup. For this output power, PAE was 20 % and we expect the peak PAE to be closer to 39 % for an output power of 37dBm as shown in Figure 2. Our work is the smallest one among the referenced works. The output power is average and output matching network needs more adjustment to increase efficiency. This work targets small cell base station applications.

The development phase requires a low-cost solution for small quantities. The hybrid PA Module comes forward as a strong solution due to its easy-post-production-tuning feature and ultra-low-cost nature when compared to the other custom MMIC based solutions.

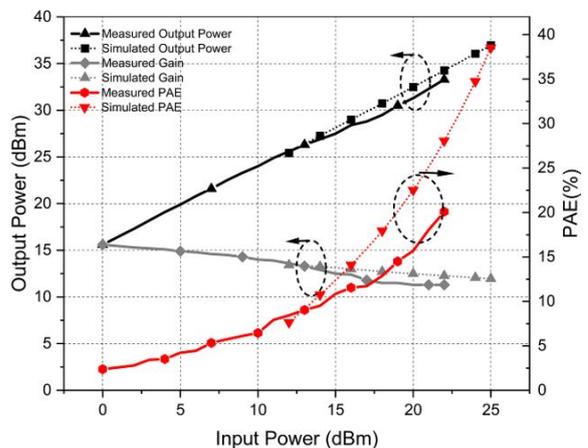


Figure 10. Measurement of output power, gain at 3.4 GHz.

Table 1. Comparison with reference products

References	Frequency (GHz)	Gain (dB)	Output Power (dBm)	Efficiency	Size (mm)
Inoue and Ebihara (2016)	3.6	24	40/32	40%/20%	8x8
Saad et al. (2010)	1.9-4.3	10	40.5	50%@3.5 GHz	65x65
Komatsuzaki et al. (2017)	3.0-3.6	12	34.2@3.5 GHz	45.9%-50.2%	78x60
Sakata et al. (2020)	3.6	30	37.3	44.7%	10x6
Barisich et al. (2015)	1.0-11.5	4	35@3.0 GHz	30%	76.2x25.4
Crescenzi et al. (2005)	1.96	27.5	44.8	45%	15.2x25.4
This work	3.4-3.6	11.3	33.2	20%	8.5x5.2

4. Conclusion

In this article, detailed design steps of a class-AB PAM are explained. The Power Amplifier Module is constructed on an 8.46 x 5.22 mm Rogers4003C laminate as a hybrid design using a GaN HEMT transistor die and 0603 sized discrete resistor, capacitor and inductors. For the design simulations, the vendor supplied compact model of CGH6008D, vendor supplied S-parameter data for the inductor, and resistor and capacitors, along with the bond wire model obtained from full-wave 3D EM simulations to account for parasitic effects of the 25 μm gold wire are used. An evaluation board was designed and fabricated along with the PA Module. Initial measurements show that more than 2W saturated output power was obtained from the PA with 11.2 dB gain and 20.1 % PAE at 3.4 GHz. S11 and S22 were measured as -12.2 dB and -7.7 dB respectively. S21 was measured as 13.4 dB at 3.5 GHz. The shunt resistor used as the stability network ensured unconditional stability of the PAM. It was verified using both small signal and large signal stability analyses.

Author Contributions

The percentage of the author(s) contributions is presented below. All authors reviewed and approved the final version of the manuscript.

	H.S.S.	B.B.T.	F.H.	H.D.
C	70			30
D	15	50	30	5
S	70			30
DCP	10	90		
DAI	20	70	5	5
L	10	70	20	
W	20	80		
CR	80	20		
SR	70	30		
PM	50	35	5	10
FA	40	20		40

C=Concept, D= design, S= supervision, DCP= data collection and/or processing, DAI= data analysis and/or interpretation, L= literature search, W= writing, CR= critical review, SR= submission and revision, PM= project management, FA= funding acquisition.

Conflict of Interest

The authors declared that there is no conflict of interest.

Ethical Consideration

Ethics committee approval was not required for this study because of there was no study on animals or humans.

Acknowledgements

This study was supported by Nero Industries Co. The authors would acknowledge the financial support of the company.

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