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Analysis of Frequency and Voltage Dependent Electrical Features of Au/Si3N4/p-GaAs (MIS) Device at Room Temperature

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Keywords

Silicon Nitride (Si3N4)
MIS Device
Capacitance
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Series Resistance
Interface States

Abstract

The investigation presented here deals with the comprehensive analysis of the C-V-f and G/ω-V-f characteristics of the Au/Si3N4/p-GaAs (MIS) device. These measurements were performed at 300 K and covered a frequency of between 10 kHz–1 MHz. The determination of the Rs was facilitated by the use of the conductance method, while the evaluation of the Nss of the MIS device was performed according to the Hill-Coleman method. A noteworthy observation concerns the significant frequency dispersion observed in the C-V-f and G/ω-V-f features of the MIS devices, particularly noticeable at low frequencies, which is attributable to the influence of Rs and Nss. Furthermore, the determination of the high-frequency Cm and Gm/ω involved measurements under both reverse and forward-biased conditions, followed by careful adjustments to mitigate the effects of Rs. This meticulous procedure culminated in the derivation of the true capacitance values inherent in semiconductor structure.

Cite

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1. INTRODUCTION

The metal-insulator semiconductor structure, frequently referred to as MIS structure, is an essential constituent in semiconductor devices used for various purposes. This structure is fundamental in MISFET/MOSFET transistors mostly used in integrated circuits for electronic devices (Sze, 1981; Rhoderick & Williams, 1988). Understanding surface physics and device functionality is crucial through the assistance of MIS structure, as semiconductor junctions are intricately linked to their surface structures (Reddy et al., 2011). The unquestionable key factor influencing the electrical, optical, and dielectric features of MIS device is the preference for an interfacial layer. This layer may form naturally at the interface between M and S, or it can be deliberately generated at the M/S interface by employing a range of techniques. Additionally, the material's thickness, permittivity and homogeneity equally play crucial roles in determining the mentioned properties (Sevgili et al., 2020; Güneşer et al., 2023). Moreover, the real MIS structure, the semiconductor-insulator interface, has many lattice defects, traps, impurities and interface states. Within the crystalline framework of a semiconductor, the presence of a foreign atom or decomposition, known as interface states, along the insulator-semiconductor boundary results in the emergence of numerous permissible energy levels within the forbidden bandgap (Nicollian & Brews, 1982). This phenomenon exerts a substantial influence on the electronic properties and behavior exhibited by the semiconductor material, manifesting in notable effects across various aspects of its functionality and performance in electronic devices.

The series resistance (R_s) of this MIS device and the density of interface trap/states (N_{ss}) are the other two crucial factors significantly impacting the measurements (Tataroğlu B. et al., 2006; Güçlü et al., 2024). The changes in capacitance within this structure typically do not rely on frequency and are anticipated to rise with

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the utilized voltage. Nonetheless, against what was expected to these changes vary significantly in practices, especially at low and medium frequencies, owing to the presence of N_{ss} at the interfacial layer, the influence of R_s, and the selection of the semiconductor interface. N_{ss} typically arise from surface features, lattice defects, surface processing and impurity in the semiconductor. Additionally, R_s arises due to a combination of factors, including the presence of ohmic and back contacts, coupling connections to the gate, and the inherent resistivity of the semiconductor material itself (Osiris et al., 2011).

Silicon nitride (Si_3N_4) constitutes a chemical compound formed through the combination of silicon and nitrogen elements, forming a stable and commonly utilized material in various applications. It exhibits ionic-covalent bonding (70% covalent) and manifests three distinct crystal structures: α, β, and c. While α- Si_3N_4 and β- Si_3N_4 can be acquired under typical nitrogen pressure, the c- Si_3N_4 structure is attainable only under extremely high pressure and temperature. Additionally, Si_3N_4 is a hard, dense refractory material (Riley, 2000). Moreover, silicon nitrate (Si_3N_4), is unremarkably used as an insulator in various electronic and semiconductor devices due to its excellent electrical insulating properties. Known for its exceptional thermal stability, robust mechanical strength and remarkable resistance to chemical corrosion, Silicon Nitride stands out as a reliable material option in a wide range of applications. These properties make it particularly suitable for use in integrated circuits and microelectronics, where reliability and performance are paramount (Buyukbas-Ulusan & Tataroğlu, 2020). Additionally, silicon nitride boasts several noteworthy properties, including but not limited to a low leakage current, a high dielectric permittivity, and a significantly larger energy gap compared to other materials (Jhansirani et al., 2016; Buyukbas-Ulusan & Tataroğlu, 2020).

In this context, the primary aim was to carry out a thorough experimental investigation of the frequency dependency of the C-V and G/ω-V properties in MIS devices, with a major emphasis on the influence of N_{ss} and R_s. In order to deepen our understanding of how N_{ss} and R_s influence these characteristics, a comprehensive series of forward and reverse bias C-V and G/ω-V measurements was meticulously performed over a broad frequency from 10 kHz to 1 MHz, as well as over a wide voltage range from -4 V to +4 V. Moreover, the C and G/ω values were carefully adjusted at elevated frequencies to mitigate the influence of R_s. In addition, careful adjustments were made to the C and G/ω values at higher frequencies to mitigate the effects of R_s, thereby establishing the authentic MIS configuration. The density of interfacial states, which is frequency dependent, was extracted from the C-V and G/ω-V datas by use of the Hill-Coleman technique (Hill & Coleman, 1980).

2. MATERIAL AND METHOD

In this work, Au/Si_3N_4/p-GaAs (MIS) structure was fabricated on p-type gallium arsenide (GaAs). The employed substrate was a 500 μm thick, (100) float zone single crystal wafer of zinc (Zn) loaded p-type gallium arsenide (GaAs) possessing a carrier concentration of $10^{17–18}$ cm^{-3}. The p-GaAs wafer was chemically cleaned in ammonium peroxide prior to the deposition process. Contaminants on the surface were eliminated by washing the wafer for one minute in a $5H_2SO_4$:H_2O_2:H_2O acidic solution, and then by etching it in an H_2O:HCl solution. After the wafer had been cleaned with 18 MΩ cm ultra-pure water, it was subjected to a dry cleaning process using pure nitrogen. Following the cleaning and etching processes, an ohmic contact was established using high-pure Au metal. A 2000 Å back contact was created on the p-GaAs wafer via thermal evaporation of Au at 375 °C under a vacuum of 3×10^{-6} Torr. Next, the wafer underwent a 7-minute annealing process in a nitrogen atmosphere at 475 °C. Following ohmic contact preparation, the wafer was heated to 400 °C in a radio frequency (RF) reactive magnetron sputtering system. Subsequently, the wafer was moved to the storage chamber for silicon nitride (Si_3N_4) film deposition. The Si_3N_4 target was used for the deposition, along with a specific Ar/O_2 reactive gas mixture, both regulated by mass flow controllers. The deposition of the Si_3N_4 thin film was performed by maintaining the wafer temperature at 200 °C and the chamber pressure at 3×10^{-6} mbar. Following the Si_3N_4 coating, a 2000 Å rectifying contact was established by thermally evaporation of Au as dots onto the Si_3N_4/p-GaAs. The dot's contact area measured at $7.85x10^{-3}$ cm^2 at a temperature of 30°C. This led to the fabrication of the Au/Si_3N_4/p-GaAs (MIS) device. The HP 4192ssoA LF impedance analyzer was utilized to measure the fabricated MIS structure across a broad frequency range at room temperature.

3. RESULTS AND DISCUSSION

Using a parallel RC circuit, the total admittance of the equivalent circuit is determined as Y= G+iωC (Sze, 1981; Nicollian & Brews, 1982; Tataroğlu A. et al., 2020). The capacitance-voltage characteristics of MIS/MOS devices to which bias voltage is applied vary according to the accumulation, depletion, and inversion regions. Furthermore, capacitance-voltage (C-V) measurements rely on the interface film's characteristics, the types and electrical features of the MIS device.

The evaluation of the C and G/ω displayed by the Au/Si_3N_4/p-GaAs (MIS) device spanned a diverse frequency spectrum, with variations observed alongside changes in bias voltage. Figure 1a and 1b display the C-V and G/ω-V graphs, respectively. It is worth noting that the C-V graphs indicate behaviour consistent with the expected C-V properties of a p-type MIS device. Distinct zones representing accumulation, depletion and inversion phases can be found in each C-V and G/ω-V plot.

Additionally, in the accumulation zone, the C and G/ω values decline as the frequency increases. Conversely, in the inversion region, the C and G/ω values remain constant regardless of frequency. The capacitance-frequency variation is accounted for by the manifestation of interface states at the semiconductor/interface, which has been identified through meticulous analysis (Türkay & Tataroğlu, 2021; Demirezen et al., 2023). The carriers' capacity to track the ac signal is immediately influenced by the specified capacitance worth, which fluctuates with variations in the dielectric constant. Observations indicate that at lower frequencies, the interface states have the tendency to effectively track the alternating current (ac) signal, thus resulting in additional contributions to the capacitance. Nevertheless, as the frequency increases, their ability to track the ac signal diminishes, thereby precluding any further augmentation of the overall capacitance.

The correlation between the capacitance, the conductance, and the frequency at several positive voltages is shown in Figure 2a and 2b. These diagrams reveal that not only C but also G/ω values decline as the voltage and frequency increase. Therefore, this observation is a proof of the presence of states of the interface. Additionally, the outcomes suggest a pronounced reliance between the measures C and G/ω concerning both the applying bias voltage and frequency.

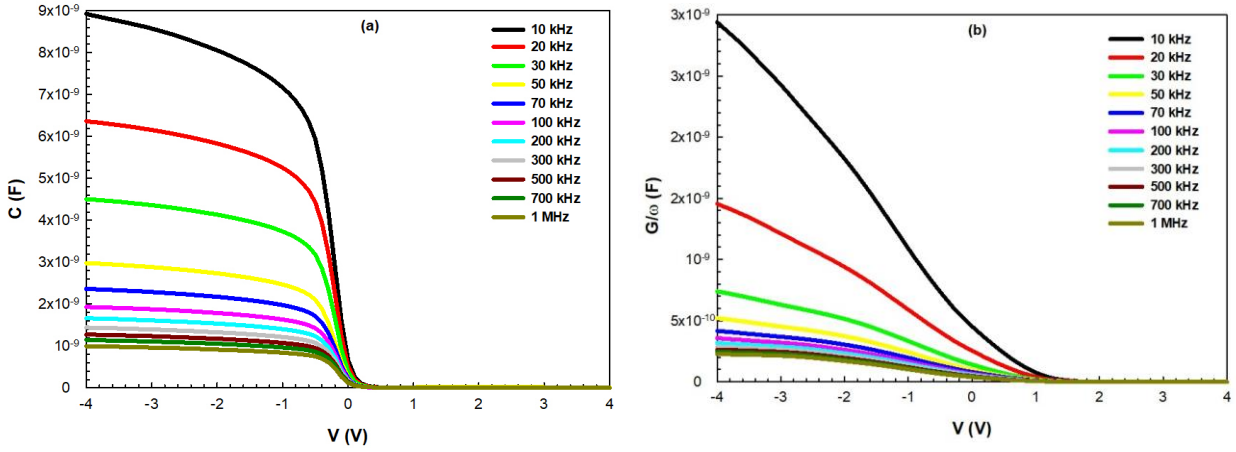

Figure 1. a) *C-V graphs,* ***b)*** *G/ω-V graphs at various frequencies*

Numerous approaches and techniques have been proposed and investigated to establish the series resistance (R_s) associated with the MIS device. This variety of methods underscores the ongoing efforts within the field to develop comprehensive and accurate means of evaluating this crucial parameter in MIS device characterization and analysis (Nicollian & Brews, 1982). In this investigation, we have utilized the approach established by Nicollian and Goetzberger. The conductivity method was invented by Nicollian and Goetzberger stands out as notably sensitive among the various techniques employed for discerning the interfacial density of states, as well as for determining the time constant of majority carriers and fluctuations in surface potential, especially in regions characterized by weak reversal and depletion (Nicollian & Goetzberger, 1967). The measurement of capacitance (C_{ma}) and conductance (G_{ma}) can be used to define the series resistance (R_s) of the MIS device. The equation for R_s is provided below,

$$R_S = \frac{G_{ma}}{(G_{ma}{}^2 + C_{ma}^2 w^2)} \tag{1}$$

where ω represents the angular frequency. Figure 3a exhibit the R_s-V graphs for a range of frequencies and Figure 3b exhibit the R_s-Log f graphs for a range of voltages. In Figure 3a, a decrease in R_s values is observed as the frequency increases, a behavior that is related to trapped charges. Additionally, Figure 3b depicts the variation in series resistance (R_s) as it fluctuates with frequency across different positive voltage levels. The graph presents a decrease in R_s values as the frequency increases, whereas the R_s values rise as the voltage increases.

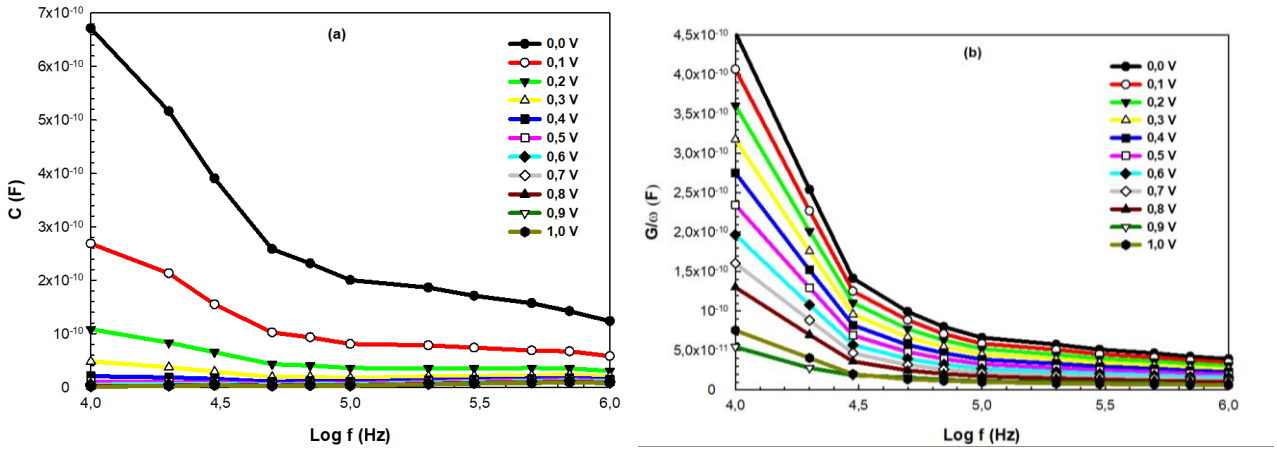

Figure 2. a) *C-Log f graphs,* ***b)*** *G/ω-Log f graphs at different positive voltages*

In cases where the series resistance (R_s) is present and notably high, it should be noted that the measured conductivity (G_m) and the measured capacitance (C_m) might not accurately represent their true values. In this case the corrected capacitance and conductivity are expressed by C_c and G_c, respectively. Consequently, in order to mitigate the impact of series resistance (R_s) in not only accumulation but also depletion zones, adjustments were made to the capacitance (C_c) and conductance (G_c) by recalibrating the measurements of C and G/ω. Subsequently, the corrected values of capacitance (C_c) and conductance (G_c) were derived using the provided equations (Nicollian & Brews, 1982),

$$C_c = \frac{\left[G_{ma}^2 + (\omega C_{ma})^2\right] C_{ma}}{a^2 + (\omega C_{ma})^2} \tag{2}$$

$$G_c = \frac{G_{ma}^2 + (\omega C_{ma})^2 a}{a^2 + (\omega C_{ma})^2} \tag{3}$$

where a is a constant that can be expressed in the form of,

$$a = G_{ma} - \left[G_{ma}^2 + (\omega C_{ma})^2\right] R_s \tag{4}$$

Figure 4a illustrates the variations in both uncorrected and corrected capacitance in response to changes in gate bias at a frequency of 1 MHz, while Figure 4b depicts the corresponding variations in both uncorrected and corrected conductance. This graphical representation provides a comprehensive comparison of the effects of gate bias on capacitance and conductance in both their uncorrected and corrected forms. Within Figure 4a, a

distinct pattern emerges wherein the corrected capacitance values exhibit a notable decrease as the voltage is progressively increased within the accumulation region. Conversely, both uncorrected and corrected capacitance values demonstrate a lack of significant alteration within the depletion and inversion regions. This observation highlights the effectiveness of the correction procedures applied in refining the accuracy of capacitance measurements, particularly in regions where changes were expected to be minimum. Furthermore, upon careful examination of Figure 4b, it becomes apparent that the corrected conductance values exhibit a discernible decline as the voltage decreases within both the accumulation and depletion zones. This trend highlights the sensitivity of the corrected measurements to variations in voltage levels across different operating regions. Additionally, the G_c/ω-V curve depicted in Figure 4b reveals a pronounced peak centered around 0 V within the depletion zone. This particular peak in the data is ascribed to the distribution pattern of charge carriers that occurs specifically at the interface between silicon nitride (Si_3N_4) and p-type gallium arsenide (p-GaAs). In other words, the interface traps can be held accountable for the corrected conductance peak.

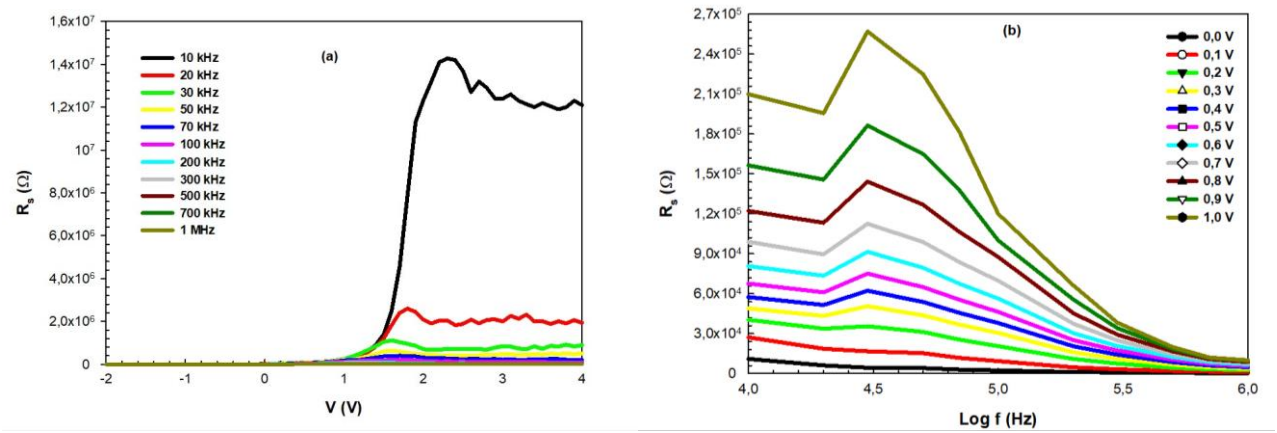

Figure 3. a) *R_s-V graphs for a range of frequencies,* ***b)*** *R_s-Log f graphs for a range of voltages*

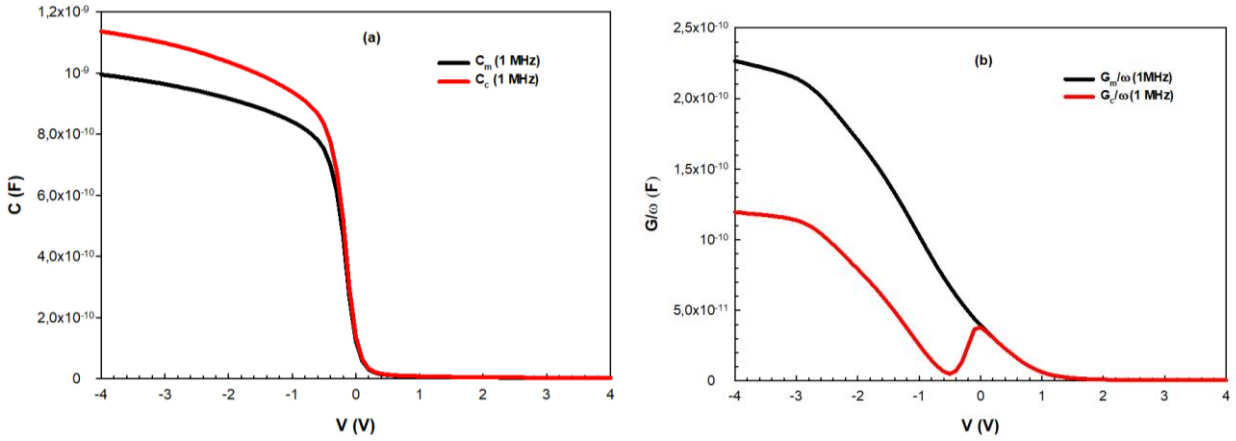

Figure 4. *The fluctuations in both the uncorrected and corrected values of* ***a)*** *C and* ***b)*** *G/ω were examined over a range of gate bias voltages at a frequency of 1 MHz*

The calculation of the interface trap/state density (N_{ss}) for the the Au/Si_3N_4/p-GaAs (MIS) structure was based on the Hill-Coleman method. With this approach, N_{ss} is expressed as follow (Hill & Coleman, 1980),

$$N_{ss} = \frac{2}{qA} \frac{(G_m/\omega)_{\max}}{((G_m/\omega)_{\max} C_{ox})^2 + (1 - C_m/C_{ox})^2)} \tag{5}$$

where A represents the area of the rectifying contact. The N_{ss} values were derived from Equation (5) and are illustrated in Figure 5. As depicted in Figure 5, as the frequency rises, there is a concurrent decrease in the N_{ss} value. This decline is a consequence of the behavior exhibited by interface charge carriers.

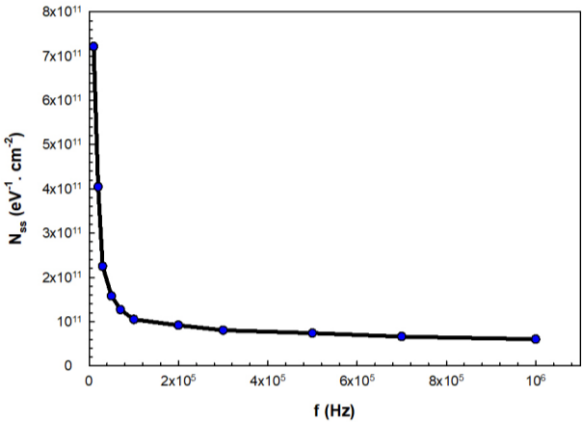

Figure 5. *The changes in N_{ss} with frequency*

4. CONCLUSION

The current research extensively delves into the analysis of the C-V-f and G/ω-V-f properties observed in the Au/Si_3N_4/p-GaAs (MIS) device. Throughout the investigation, careful attention was paid to the impact of R_s on the C and G/ω parameters, ensuring their accurate representation. It was noted that the R_s values exhibited a decreasing trend with the increase in frequency, while conversely, they showed an upward trend with increasing voltage levels. Hill-Coleman method was used to evaluate the N_{ss}. The obtained results underscore the significant impact of both N_{ss} and R_s on the electrical features of the device. Particularly noteworthy is the inverse relationship observed between N_{ss} values and frequency, indicating a reduction in interface state density as frequency increases. This phenomenon may be ascribed to the behavior of interface charge carriers, shedding light on the intricate dynamics governing the device's performance.

CONFLICT OF INTEREST

The author declares no conflict of interest.

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