HITTITE JOURNAL OF SCIENCE AND ENGINEERING

e-ISSN: 2148-4171
Volume: 11 • Number: 4
December 2024

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Article Information
Article Type: Research Article
Doi: https://doi.org/10.17350/HJSE19030000343
Received: 17.08.2024
Accepted: 04.10.2024
Published: 31.12.2024

Cite As
Sakaci B, Ozenli D. Noise Analysis For Active Element Based Capacitor Multipliers. Hittite J Sci Eng. 2024;11(4):157-167.

Peer Review: Evaluated by independent reviewers working in at least two different institutions appointed by the field editor.
Ethical Statement: Not available.
Plagiarism Checks: Yes - iThenticate
Conflict of Interest: Authors approve that to the best of their knowledge, there is not any conflict of interest or common interest with an institution/organization or a person that may affect the review process of the paper.

CRediT AUTHOR STATEMENT
Burak SAKACI: Circuit Design, Methodology, Layout Design, Simulation, Writing- original draft. **Deniz OZENLI:** Data curation, Visualization, Investigation, Writing- original draft.

Noise Analysis For Active Element Based Capacitor Multipliers

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Abstract

In this study, comprehensive noise analyses and optimization of two different capacitance multiplier structures have been presented. Capacitor multipliers, essential in low frequency applications due to capacitors' significant chip area requirement, play a significant role in high precision analog circuits. Noise impacts such filters by reducing the signal to noise ratio (SNR), increasing phase noise, and potentially causing distortion, which is critical in applications requiring high accuracy and stability, such as biomedical instrumentation, communication systems, and precision measurement devices. Therefore, thorough analysis and optimization of filter noise characteristics are essential for reliable operation in sensitive applications. Two capacitor multiplier structures are analyzed: the Multiple Output Voltage Differencing Transconductance Amplifier (MO-VDTA) based and the Multiple Output Current Differencing Transconductance Amplifier (MO-CDTA) based structures. The multiplication factor of the capacitor multiplier in basis of MO-VDTA varies between 120 and 750, depending on the I_B value.
This variation allows the cutoff frequency of the applied filter to change between 2 kHz and 12.4 kHz. The MO-CDTA based structure's multiplication factor varies between 400 and 1250 by changing the V_{GS} voltage of the external PMOS. This structure has been used in a 2nd order low pass filter, with the cutoff frequency varying between 23.6 kHz and 91 kHz in conjunction with multiplication factor changing. In this respect, comprehensive noise analyses of the filter applications of these two structures have been examined to ensure reliable and efficient operation in sensitive applications.

Keywords: Multiplication Factor, Capacitor Multiplier Multiple Output Voltage Differencing Transconductance Amplifier (MO-VDTA), Multiple Output Current Differencing Transconductance Amplifier (MO-CDTA), Noise Analysis

INTRODUCTION

Nowadays, modern analog circuit designs necessitate high capacitance values for a wide range of applications such as subhertz, speech, ultrasound, and biomedical fields. These applications demand substantial capacitance to function effectively specific frequency interval (1,2). Capacitor multipliers are used to achieve these high capacitance values at low production costs and in small chip areas (3,4). Capacitor multiplier structures can operate in two different modes: Current-mode and voltage-mode. In the current-mode capacitor multiplier equation, C_M represents the multiplied capacitance, C_B denotes the base capacitance, and "k" indicates the multiplication factor. This equation is expressed in the literature as $C_M = (1+k). C_B$ (5). Numerous active building blocks are employed to create efficient capacitor multiplier designs (1-18). Wearable technology, including smartwatches, wireless headphones, and biomedical devices, is a prominent market trend. Biomedical signals, with their low voltage levels, require filtering for human health compatibility (19,21). These filters often use large capacitors to achieve low frequency characteristics, as referred to (22). Ultrasound applications, such as food drying, distance measurement, and biomedical uses, are also drawing attention (23,25). Reference (26) also includes these operating frequency ranges. In this point of view, this study will discuss extended noise analyses of capacitor multiplier based filters suitable for these frequency ranges, with their role in signal processing depicted in Figure 1.

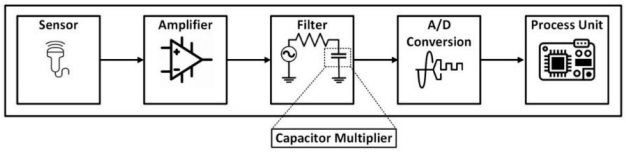

Figure 1 Capacitor multipliers in signal processing

Figure 1 highlights the crucial role of capacitors in filters. Noise analysis in filters is essential for optimizing performance and reliability by improving signal to noise ratios and reducing errors (27). Thanks to the noise analyses conducted on filters, component selection, design, and configurations are informed, enabling the design of filters that comply with standards, especially for biomedical and ultrasound applications (28).

This study presents extended noise analyses and optimizations for two filters using different active element blocks. The cutoff frequencies for 2nd order low pass filters with MO-VDTA and MO-CDTA structures are tunable from 2 kHz to 12.4 kHz and 23.6 kHz to 91 kHz, respectively, based on TSMC 0.18 µm CMOS technology. The study covers active element based capacitor multipliers, filter applications, noise optimization, and results using LT-Spice and Magic Layout Environment. Future work is also outlined.

MATERIAL AND METHODS

This section describes the capacitor multiplier structures used in this study. Capacitor multipliers have been implemented in the literature using various active elements. While some are realized with OTAs and current conveyors (29,30), others are implemented with different active elements. Some of them are valuable for high capacitance, variable capacitance, and low frequency operations, offering flexibility in filter design and optimization (12,31,32). In this study, MO-VDTA and MOCDTA based capacitor multipliers will be focused on this work, with all simulations performed with LT-Spice and Magic VLSI.

All simulation results in this study are based on layouts created using Magic VLSI. Figure 2 shows the MO-VDTA based capacitor multiplier structure, which occupies an area of 36.36 µm × 21.96 µm. Additionally, Figure 3 shows the MO-CDTA capacitor multiplier structure, which occupies an area of 176.76 µm × 136.71 µm.

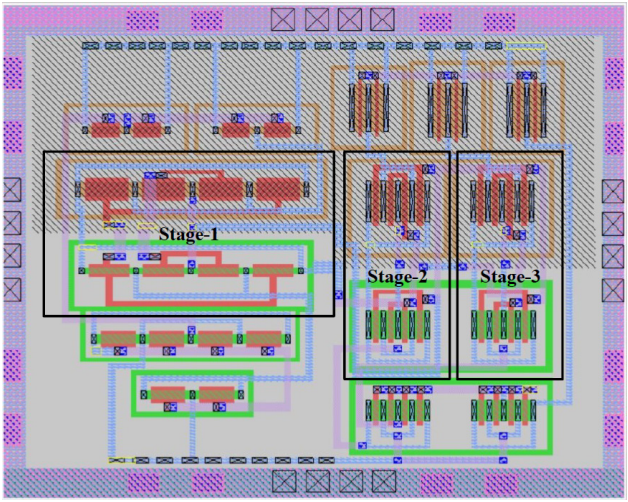

Figure 2 Layout of MO-VDTA Based Capacitance Multiplier

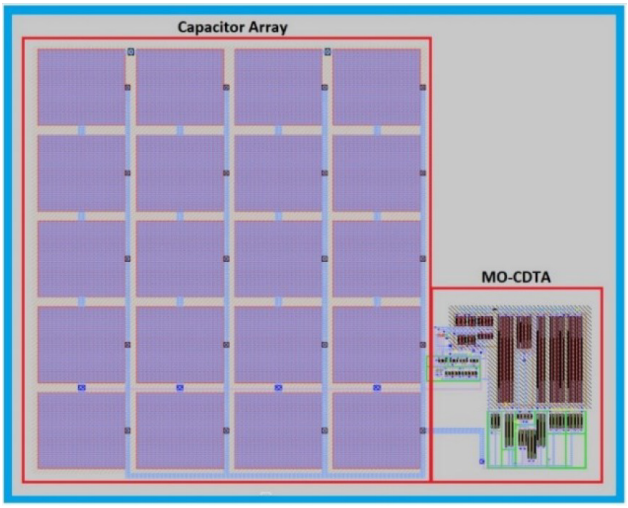

Figure 3 Layout of MO-CDTA Based Capacitance Multiplier

The VDTA structure, crucial for analog circuit design, traditionally includes two OTA stages (12,33,34). The MO-VDTA extends this with additional OTA stages, providing higher gain and suitability for current mode capacitive multipliers requiring large multiplication factors. The proposed MO-VDTA based multiplier has three OTA stages, seven terminals, and offers high impedance for easy interconnection, with V_P and V_N as differential inputs and V_Z as the output (35).

$$\begin{bmatrix} I_Z \\ I_{X1}+ \\ I_{X1}- \\ I_{X2}+ \\ I_{X2}- \end{bmatrix} = \begin{bmatrix} \gamma_1 G_{m1} & -\gamma_1 G_{m1} & 0 \\ 0 & 0 & \gamma_1 G_{m2} \\ 0 & 0 & -\gamma_2 G_{m2} \\ 0 & 0 & \gamma_3 G_{m3} \\ 0 & 0 & -\gamma_3 G_{m3} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad (1)$$

Current mode capacitor multipliers utilize a feedback mechanism to scale base capacitance (7). Figure 4 illustrates a compact multiplier structure based on multioutput VDTA using X-terminal currents. Despite the rise in power consumption, silicon area, and design complexity, additional OTA stages can be added to enhance the "k" factor.

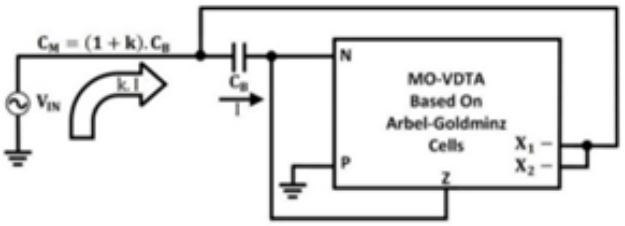

Figure 4 Capacitor multiplier based on MO-VDTA

Equations (2) and (3) describe the input impedance and multiplication factor of the proposed structure, while equation (5) provides the cut off frequency of a 1st order low pass filter. Tracking errors from the MO-VDTA's characteristic matrix, shown in equation (1), can be safely eliminated, so that γ coefficients are nearly 1 up to 10 MHz for the properly dimensioning in basis of TSMC 0.18µm technology. For low frequency applications up to 100 kHz, equations in (2) and (3) simplify the calculations for multiplication factor and cut off frequency as given in equations (4) and (5).

$$Z = \frac{sC_B + \gamma_1 G_{m1}}{sC_B\left(\gamma_1 G_{m1} + \gamma_2 G_{m2} + \gamma_3 G_{m3}\right)} \quad (2)$$

$$Z \cong \frac{G_{m1}}{sC_B\left(G_{m1} + G_{m2} + G_{m3}\right)} \quad (3)$$

$$k \cong \frac{G_{m1} + G_{m2} + G_{m3}}{G_{m1}} \quad (4)$$

$$\omega_{cut-off} \cong \frac{1}{kRC_B} \quad (5)$$

To attain a high multiplication factor, the first OTA stage's transconductance gain is kept lower than that of later stages, with the parameter "k" controlled by G_{M1}. Thus, transistors in the first OTA stage have smaller aspect ratios compared to those in the subsequent stages (6). For the first Arbel Goldminz cell, I_D in equation of (6) equals I_B /2, while in the second and third cells, it is approximately I_C/ 2. Figure 5 illustrates the OTA stages, where each transistor size is selected meticulously.

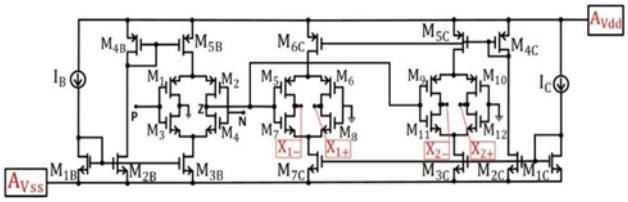

Figure 5 Transistor level of MO-VDTA

Table 1 MO-VDTA Transistors' dimensions

TRANSISTOR	Dimensions		TRANSISTOR	Dimensions	
	W	L		W	L
M_{1B}, M_{2B}, M_{3B}	0.6 µm	5 µm	M_1, M_2	1 µm	6 µm
M_{4B}, M_{5B}	1 µm	2 µm	M_3, M_4	0.3 µm	6 µm
M_{4C}	7 µm	0.18 µm	M_5, M_6, M_9, M_{10}	6 µm	0.36 µm
M_{5C}	8 µm	0.18 µm	M_{1C},M_{2C},M_{3C},M_{7C}	3 µm	0.36 µm
M_{6C}	8 µm	0.18 µm	M_7, M_8,M_{11}, M_{12}	4 µm	0.36 µm

$$g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D} \tag{6}$$

The OTA cell gains are adjusted via bias currents I_B =25 nA and I_C =60 µA, resulting in the 1st OTA stage having a lower gain. The transconductance gains are G_{M1} = 250 nS and G_{M2} = G_{M3} = 110 µS.

The conventional Current Differencing Transconductance Amplifier (CDTA) is a key element in analog circuits (36,37). The MO-CDTA enhances the CDTA by adding extra output stages to the DO-OTA block, providing increased flexibility and suitability for high capacitance and current mode applications. The proposed MO-CDTA based capacitor multiplier uses three OTA stages to simplify the structure and reduce power consumption. The MO-CDTA's multiple outputs and amplified transconductance gain, as shown in equation (7), facilitate achieving a higher multiplication factor.

$$\begin{bmatrix} V_P \\ V_N \\ I_Z \\ I_{X1}+ \\ I_{X1}- \\ I_{X2}+ \\ I_{X2}- \\ I_{X3}+ \\ I_{X3}- \\ I_{X4}+ \\ I_{X4}- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & +G_{m1} \\ 0 & 0 & 0 & -G_{m1} \\ 0 & 0 & 0 & +G_{m2} \\ 0 & 0 & 0 & -G_{m2} \\ 0 & 0 & 0 & +G_{m3} \\ 0 & 0 & 0 & -G_{m3} \\ 0 & 0 & 0 & +G_{m4} \\ 0 & 0 & 0 & -G_{m4} \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_X \\ V_Z \end{bmatrix} \tag{7}$$

Equation (7) omits terminal parasitics for clarity. Figure 6 presents the transistor level implementation of the MO-CDTA, which is fully tunable via bias currents. Adding more output stages increases transconductance gain but also complexity and power consumption. The gain of each stage is defined by equation (8).

$$G_M \cong B\sqrt{\mu_n C_{OX} I_C \left(\frac{W}{L}\right)_{9,10}} \tag{8}$$

In equation (8), B denotes the ratio of $\left(\frac{W}{L}\right)_{4C}/\left(\frac{W}{L}\right)_{5C}$ It is evident that the main factors affecting the gain are the bias current I_C and the W/L ratios of the relevant transistors. The transistor size of MO-CDTA is selected with sensitivity. Table 2 representes transistor sizes of MO-CDTA.

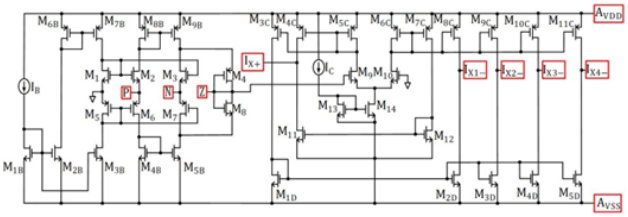

Figure 6 Transistor level of MO-CDTA

Table 2 MO-CDTA Transistors' dimensions

TRANSISTOR	Dimensions		TRANSISTOR	Dimensions	
	W	L		W	L
M_1B	1µm	0.36µm	M_{3C}, M_{4C}, M_{7C}, M_{8C} M_{9C}, M_{10C}, M_{11C}	54µm	0.36µm
M_{2B}, M_{3B}, M_4B, M_{5B}	2µm	0.36µm	M_{5C}, M_{6C}, M_{11}, M_{12}	20µm	0.36µm
M_{6B}	6µm	0.72µm	M_{13}	10µm	0.36µm
M_{7B}, M_{8B}, M_{9B}, M_5, M_6	6µm	0.36µm	M_{14}	18µm	0.36µm
M_1, M_2, M_3, M_8	1.5µm	0.36µm	M_{1D}, M_{2D}, M_{3D}, M_{4D}, M_{5D}	9µm	0.36µm
M_4, M_7, M_9, M_{10}	3µm	0.36µm			

The proposed design operates as a current mode capacitor multiplier, similar to the one described in the previous section. This is illustrated in Figure 7.

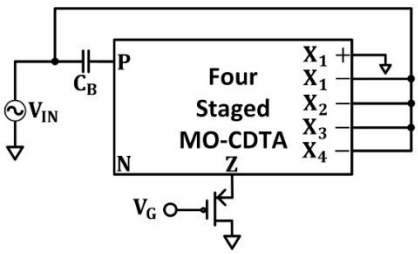

Figure 7 Capacitor multiplier based on MO-CDTA

The resistor value R_{MOS} in Figure 7 reflects the resistive properties of the PMOS transistor in the triode region, connected to the Z terminal of the multiplier

$$R_{MOS} \cong \frac{1}{k_P \frac{W}{L}(V_{SG} - |V_T|)} \tag{9}$$

In this setup, the control voltage V_{GS} adjusts resistance, enabling electronic tuning of the capacitance multiplier as shown in Figure 7. Bias currents I_B and I_C ensure flexibility, while the output stages are crucial for achieving the desired multiplication factor. For ultrasonic applications, equation (10) can be simplified as equation (11), with the MO-CDTA's characteristic matrix and terminal parasitics as detailed.

$$Z \cong \frac{(R_{XP-})(1+sC_B R_P)}{sC_B((R_{XP-})+4R_P+4G_M(R_{MOS}//R_{ZP})(R_{XP-}))+4} \quad (10)$$

To simplify the impedance formula in the frequency range from 10 kHz to 1 MHz, terminal parasitics are neglected, resulting in the impedance formula as given in Equation 11.

$$Z \cong \frac{1}{sC_B+4sC_B G_m R_{MOS}} \quad (11)$$

Furthermore, the multiplication factor "k" for the proposed architecture is defined as shown in equation (12).

$$k \cong 1+4G_m R_{MOS} \quad (12)$$

Active element based capacitor multipliers, including MO-VDTA and MO-CDTA structures, offer significant benefits in filter design across various fields. In biomedical applications, they enable high precision filters for accurate signal processing. For speech processing, their adaptability enhances voice clarity and noise reduction. In ultrasound, they provide high frequency filters that improve signal handling and resolution. Following explains explores filter structures using MO-VDTA, applicable for low frequency usage in biomedical and speech filtering with roll off frequencies from several kHz to over 20 kHz. A 2nd order filter based on MO-VDTA is illustrated in Figure 8.

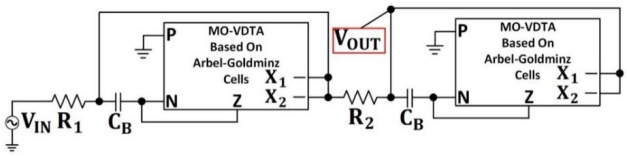

Figure 8 2nd order low pass filter based on MO-VDTA

The equations for the filter structure created with the MO-VDTA configuration are provided below, respectively:

$$\frac{V_{LP}}{V_{IN}} \cong \frac{1}{s^2 \frac{C_B^2 R_1 R_2 (G_{m1}+G_{m2}+G_{m3})^2}{G_{m1}^2} + s\frac{C_B(2R_1+R_2)(G_{m1}+G_{m2}+G_{m3})}{G_{m1}} + 1} \quad (13)$$

$$\omega_0 \cong \sqrt{\frac{G_{m1}^2}{C_B^2 R_1 R_2 (G_{m1}+G_{m2}+G_{m3})^2}} \quad (14)$$

$$Q \cong \sqrt{\frac{R_1 R_2}{(2R_1+R_2)^2}} \quad (15)$$

$$S_{G_{m1}}^{\omega_0} \cong \frac{G_{m2}+G_{m3}}{G_{m1}+G_{m2}+G_{m3}}, S_{G_{m2}}^{\omega_0} \cong \frac{-G_{m2}}{G_{m1}+G_{m2}+G_{m3}}, S_{G_{m3}}^{\omega_0} \cong \frac{-G_{m3}}{G_{m1}+G_{m2}+G_{m3}}, S_{R_1,R_2}^{\omega_0} \cong -\frac{1}{2}, S_{C_B}^{\omega_0} \cong -1 \quad (16)$$

$$S_{R_1}^{Q} \cong -\frac{2R_1-R_2}{4R_1+2R_2}, S_{R_2}^{Q} \cong \frac{2R_1-R_2}{4R_1+2R_2} \quad (17)$$

When the multiplication factor ranges from 120 to 750, the cutoff frequency of the 2nd order filter varies between 2 kHz and 12.4 kHz, as shown in Figure 9. During this operation, the filter's power consumption is approximately 840 µW. For a 1st order filter, the cut off frequency ranges from 2.6 kHz to 15.8 kHz, making these frequency ranges suitable for the specific applications.

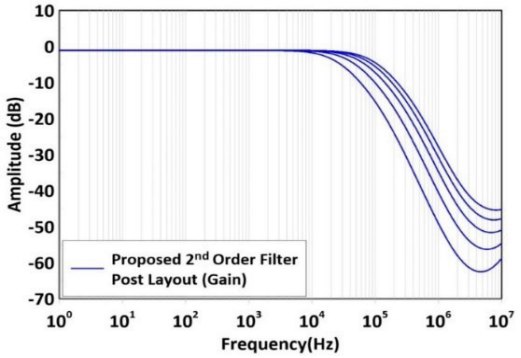

Figure 9 Gain response of 2nd order low pass filter based on MO-VDTA varying with different I_B (I_B= 25 nA to 250 nA, I_C = 60µA and R_{IN} = 50 kΩ).

To apply the proposed multiplier structure in ultrasound applications, both 1st order and 2nd order filters can be utilized. Figure 10 shows a 2nd order filter created with the MO-CDTA structure, which is electronically tunable and suitable for both low frequency and ultrasonic applications.

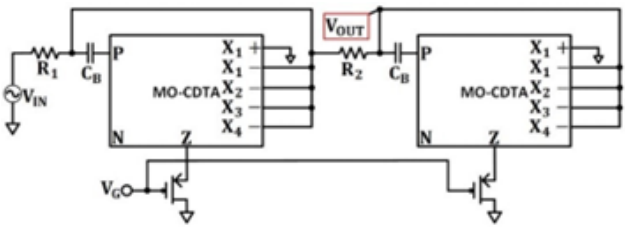

Figure 10 2nd order low pass filter based on MO-CDTA

For ultrasonic applications, filter structures are designed to operate between 20 kHz and 100 kHz with adequate suppression (22). The proposed capacitor multiplier circuit, with a multiplication factor from 400 to 1250, is integrated into a 2nd order filter as shown in Figure 10. By setting $R_1 = R_2$=1 kΩ, the cut off frequency ranges from 23.6 kHz to 91 kHz, as illustrated in Figure 11, with V_{GS} varying from -0.5 V to -0.9 V in 0.1 V steps. The filter's power consumption is approximately 1.17 mW.

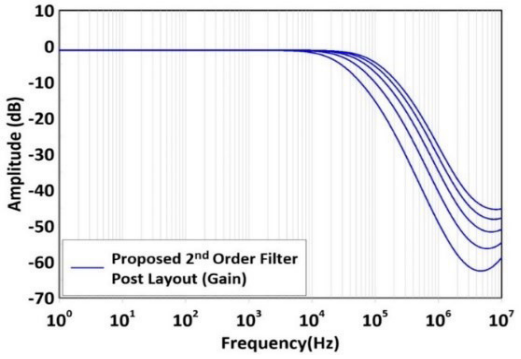

Figure 11 Gain response of 2nd order low pass filter based on MO-VDTA varying with different VGS (VGS= -0.5V to -0.9V).

Equations (18) and (19) provide the transfer functions for the low pass filters, including simplifications for parasitic effects.

The subsequent analysis describes the observed behavior of the 2nd order low pass filter. The behavior observed for the 1st and 2nd order low pass filter are as follows:

$$\frac{V_{OUT}}{V_{IN}} \cong \frac{R_{XP-}}{4R_1 + (R_{XP-}) + sC_B R_1 (R_{XP-})(1 + 4G_m (R_{MOS} // R_{ZP}))} \cong \frac{1}{1 + sC_B R_1 (1 + 4G_m R_{MOS})} \quad (18)$$

$$\frac{V_{OUT}}{V_{IN}} \cong \frac{1}{s^2 R_1 R_2 C_B^2 (1 + 4G_m R_{MOS})^2 + sC_B (R_1 + R_2)(1 + 4G_m R_{MOS}) + 1} \quad (19)$$

The cut off frequency and quality factor are calculated from equations (20), which are based on the transfer functions in equations (18) and (19). Furthermore, for the 2nd filter intended for ultrasound applications, sensitivity analyses for ω0 and Q are related to the dimensions of transistors and passive components, as outlined below:

$$\omega_0 \cong \sqrt{\frac{1}{C_B^2 R_1 R_2 (1 + 4G_m R_{MOS})^2}}, Q \cong \sqrt{\frac{R_1 R_2}{(2R_1 + R_2)^2}} \quad (20)$$

$$S_{C_B}^{\omega_0} \cong -1,\ S_{R_1, R_2}^{\omega_0} \cong -\frac{1}{2},\ S_{G_m, R_{MOS}}^{\omega_0} \cong -\frac{4G_m R_{MOS}}{4G_m R_{MOS} + 1} \quad (21)$$

$$S_{R_1}^{Q} \cong -\frac{2R_1 - R_2}{4R_1 + 2R_2},\ S_{R_2}^{Q} \cong \frac{2R_1 - R_2}{4R_1 + 2R_2} \quad (22)$$

RESULTS AND DISCUSSION

Noise analysis and optimization in the 2nd order low pass filters with capacitor multiplier structures are critical, particularly for biomedical and power ultrasound applications. Filters with cut off frequencies from 10 kHz to 100 kHz require careful optimization to mitigate active noise sources, such as flicker and thermal noise, which affect performance. Flicker noise is prominent at lower frequencies, while thermal noise increases at higher frequencies. Effective noise management involves optimizing transistor dimensions and passive components to improve the signal to noise ratio and meet performance standards. Essential mathematical equations for flicker and thermal noise analysis are detailed below (38-41).

$$\overline{i_n^2} = 4k\gamma T g_m \ [A^2/\mathrm{Hz}] \rightarrow \text{Thermal Noise} \quad (23)$$

$$\overline{i_n^2} = \frac{KFI_D}{C_{OX} L^2} \frac{1}{f} \ [A^2/\mathrm{Hz}] \rightarrow \text{Flicker (1/f) Noise} \quad (24)$$

To analyze noise in the MO-VDTA based filter, identify the key noise sources at each terminal using the characteristic matrix (1). Integrating these sources into the model is visualized, as shown in the Figure 12.

The transistor level MO-VDTA structure in Figure 5 influences the noise contributions at terminals as shown in Figure 12. Simplified equations, excluding some secondary transistor effects, lead to the equivalent noise at the 2nd order filter input, as given in Equation 25.

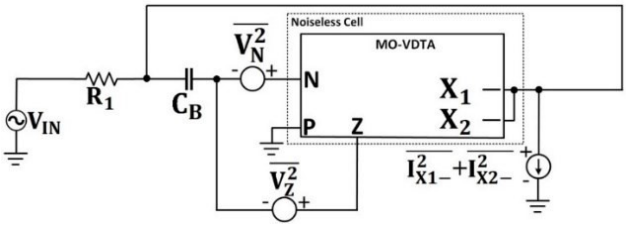

Figure 12 Noise sources of investigated filter

$$\overline{V_{IRN}^2} \cong 2\left(\overline{V_N^2} + \overline{V_P^2}\right) + R_1^2 (\overline{i_{X1-}^2} + \overline{i_{X2-}^2}) + R_2^2 (\overline{i_{X1-}^2} + \overline{i_{X2-}^2}) \quad (25)$$

For thorough noise analysis, individual contributions of noise sources in Equation 25 must be evaluated. The effects of noise at the N and Z nodes will be analyzed separately, while the grounded P node is excluded. Figure 13 shows the configuration with noise sources at the N and Z nodes.

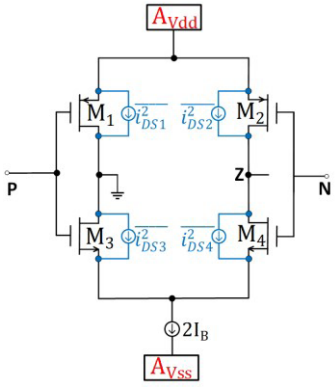

Figure 13 Noise sources of 1st stage

Referring to Figure 13, the noise equations dependent on voltage for the N and Z nodes are specified by Equation 26 and Equation 27, respectively.

$$\overline{V_N^2} \cong \frac{\overline{i_{DS1}^2} + \overline{i_{DS2}^2} + \overline{i_{DS3}^2} + \overline{i_{DS4}^2}}{g_{m1}^2} \quad (26)$$

$$\overline{V_Z^2} \cong \frac{\overline{i_{DS1}^2} + \overline{i_{DS2}^2} + \overline{i_{DS3}^2} + \overline{i_{DS4}^2}}{g_{m3}^2} \quad (27)$$

Figure 14 shows that noise from the second and third stages is mainly treated as current sources. Equations 28 and 29 are derived from this analysis.

$$\overline{i_{X1-}^2} \cong \overline{i_{DS5}^2} + \overline{i_{DS6}^2} + \overline{i_{DS7}^2} + \overline{i_{DS8}^2} \quad (28)$$

$$\overline{i_{X2-}^2} \cong \overline{i_{DS9}^2} + \overline{i_{DS10}^2} + \overline{i_{DS11}^2} + \overline{i_{DS12}^2} \quad (29)$$

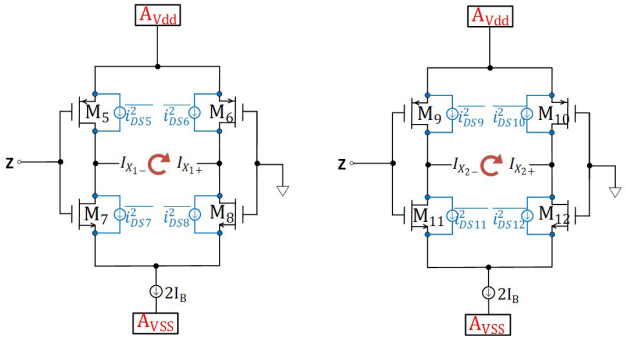

Figure 14 Noise sources of 2st and 3rd stages

The "I" equations account for both flicker and thermal noise, as shown in Equations 23 and 24. Parasitic effects are excluded. Extending Equations 26 through 29 leads to Equation 30.

$$\overline{V_{IRN}^2} \cong \begin{bmatrix} 2\left(\frac{\overline{i_{DS1}^2}+\overline{i_{DS2}^2}+\overline{i_{DS3}^2}+\overline{i_{DS4}^2}}{g_{m1}^2}+\frac{\overline{i_{DS1}^2}+\overline{i_{DS2}^2}+\overline{i_{DS3}^2}+\overline{i_{DS4}^2}}{g_{m3}^2}\right)+\dots \\ R_1^2\left(\overline{i_{DS5}^2}+\overline{i_{DS6}^2}+\overline{i_{DS7}^2}+\overline{i_{DS8}^2}+\overline{i_{DS9}^2}+\overline{i_{DS10}^2}+\overline{i_{DS11}^2}+\overline{i_{DS12}^2}\right)+\dots \\ R_2^2\left(\overline{i_{DS5}^2}+\overline{i_{DS6}^2}+\overline{i_{DS7}^2}+\overline{i_{DS8}^2}+\overline{i_{DS9}^2}+\overline{i_{DS10}^2}+\overline{i_{DS11}^2}+\overline{i_{DS12}^2}\right) \end{bmatrix} \quad (30)$$

Equation 30 indicates that multiple variables affect the equivalent noise at the input. Key factors determining the equivalent noise include the transconductance g_m of the second and third stages and the bias current I_C, with the bias current I_B of the first stage having a lesser impact due to its nA level. The noise contributions from I_C were tested at four levels, showing approximately 10% variation, as depicted in Figure 15. The analysis and optimization will focus on these parameters to enhance filter performance.

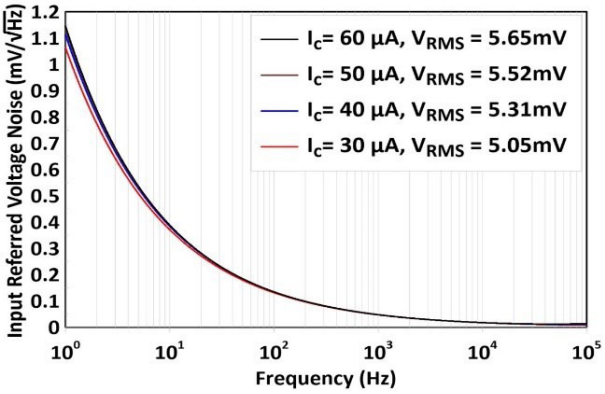

Figure 15 Input referred noise @ different I_C values

Following the analysis of I_C effects on noise, the focus shifts to gm. By halving the W/L ratio achieved by doubling the L value of transistors in the and third stages, g_m is reduced, lowering filter noise. Variations in gm and I_C are shown in the Figure 16 and Table 3

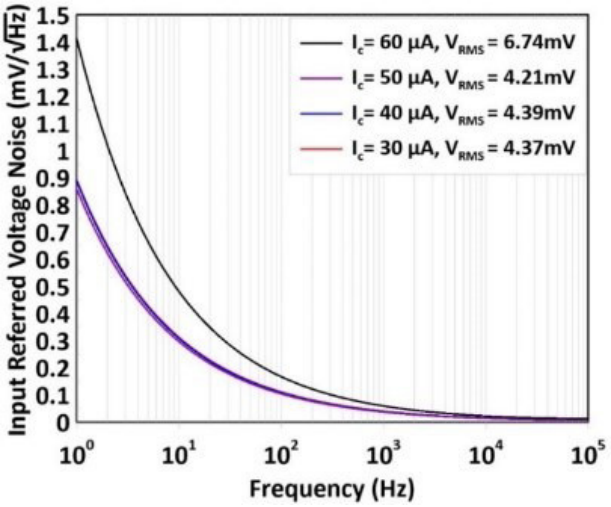

Figure 16 Input referred noise @ different I_C values with $g_m/2$

Table 3 displays the impact of g_m and I_C on noise. For NMOS transistors, g_m values are 376 µS and 105 µS; for PMOS, 220 µS and 139 µS. Variations in g_m and I_C significantly affect noise levels. However, decreased noise can worsen filter characteristics; at optimal settings, reducing noise by 40% results in a 20% change in cut off frequency. Depending on the application, trade-offs between noise reduction and filter performance must be considered, with potential exploration of alternative methods and variables for optimization.

To analyze noise for the MO-CDTA filter, dominant noise sources at each terminal, based on the characteristic matrix (7), must be identified and incorporated into the model. The block diagram showing these noise sources is illustrated in Figure 17.

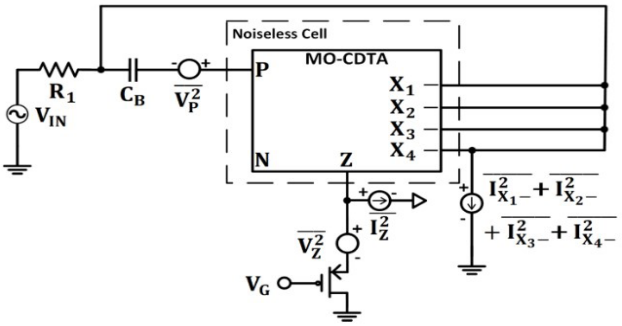

Figure 17 Noise sources of investigated filter

To determine the input referred voltage noise, derive the general equation for the equivalent input noise. Equations 31 and 32 provide the formulations for calculating this input referred voltage noise.

$$\overline{V_{IRN(1^{st})}^2} \cong \overline{V_P^2}+\overline{V_Z^2}+R_1^2\left(\overline{i_{X1-}^2}+\overline{i_{X2-}^2}+\overline{i_{X3-}^2}+\overline{i_{X4-}^2}+\overline{i_Z^2}\right) \quad (31)$$

$$\overline{V_{IRN(2^{nd})}^2} \cong 2\left[\overline{V_P^2}+\overline{V_Z^2}+R_1^2\left(\overline{i_{X1-}^2}+\overline{i_{X2-}^2}+\overline{i_{X3-}^2}+\overline{i_{X4-}^2}+\overline{i_Z^2}\right)\right] \quad (32)$$

To analyze the noise of the structure, assess the impact

Table 3 Effects of gm and I_c values on noise performance

g_m Values	I_c(μA)	Input Referred Voltage Noise	fCUT	dB Loss	g_m Values	I_c(μA)	Input Referred Voltage Noise	fCUT	dB Loss
g_m	60	10.13mV	2kHz	-2.6dB	$g_m/\sqrt{2}$	60	9.18mV	12.4kHz	-33dB
g_m	50	9.18mV	2.3kHz	-3dB	$g_m/\sqrt{2}$	50	6.39mV	7.2kHz	-16dB
g_m	40	7.67mV	5kHz	-8.2dB	$g_m/\sqrt{2}$	40	6.81mV	2.4kHz	-1dB
g_m	30	6.28mV	9.6kHz	-11dB	$g_m/\sqrt{2}$	30	6.19mV	3kHz	-1.2dB

of each transistor's noise on the input and output ports, as shown in Figure 17. The calculation, based on the transistors in Figure 18, evaluates the current impact on output terminals. For simplification, only significant transistors were included in the analysis, excluding others to manage complexity and focus on those with substantial effects.

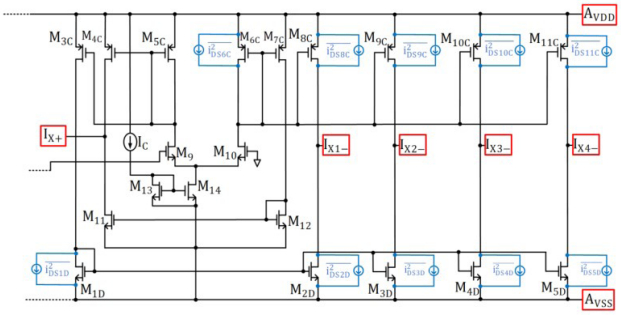

Figure 18 Noise sources of MO-CDTA

The noise impact on the output terminals is depicted by Equation 33, 34,35,37 and 37 as shown in Figure 18.

$$\overline{i^2_{OUT(OTA)}} \cong \overline{i^2_{DS5C}} + \overline{i^2_{DS6C}} + \overline{i^2_{DS9}} + \overline{i^2_{DS10}} \tag{33}$$

$$\overline{i^2_{X1-}} \cong \overline{i^2_{DS8C}} + \overline{i^2_{DS2D}} + \left(\frac{g_{m2D}}{g_{m1D}}\right)^2 \overline{i^2_{DS1D}} + \left(\frac{g_{m8C}}{g_{m6C}}\right)^2 \overline{i^2_{OUT(OTA)}} \tag{34}$$

$$\overline{i^2_{X2-}} \cong \overline{i^2_{DS9C}} + \overline{i^2_{DS3D}} + \left(\frac{g_{m3D}}{g_{m1D}}\right)^2 \overline{i^2_{DS1D}} + \left(\frac{g_{m9C}}{g_{m6C}}\right)^2 \overline{i^2_{OUT(OTA)}} \tag{35}$$

$$\overline{i^2_{X3-}} \cong \overline{i^2_{DS10C}} + \overline{i^2_{DS4D}} + \left(\frac{g_{m4D}}{g_{m1D}}\right)^2 \overline{i^2_{DS1D}} + \left(\frac{g_{m10C}}{g_{m6C}}\right)^2 \overline{i^2_{OUT(OTA)}} \tag{36}$$

$$\overline{i^2_{X4-}} \cong \overline{i^2_{DS11C}} + \overline{i^2_{DS5D}} + \left(\frac{g_{m5D}}{g_{m1D}}\right)^2 \overline{i^2_{DS1D}} + \left(\frac{g_{m11C}}{g_{m6C}}\right)^2 \overline{i^2_{OUT(OTA)}} \tag{37}$$

Figure 19.a illustrates the transistors affecting noise at the P terminal, with the equivalent noise given by Equation 38. For the Z terminal, Figure 19.b and MOSFET noise equations (23,24) lead to the derivation of Equations 39 and 40, which describe the associated noise contributions.

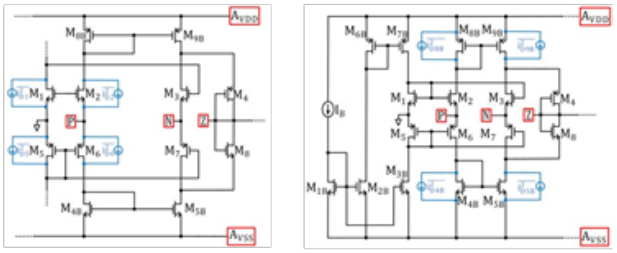

Figure 19 Noise sources visualization for input referred noise effects' calculations at a) P terminal b) P and Z Terminals

$$\overline{V_P^2} \cong \frac{\overline{i^2_{D1}} + \overline{i^2_{D2}} + \overline{i^2_{D5}} + \overline{i^2_{D6}}}{g^2_{m1}} \tag{38}$$

$$\overline{i_Z^2} \cong \overline{i^2_{DS5B}} + \overline{i^2_{DS9B}} + \left(\frac{g_{m5B}}{g_{m4B}}\right)^2 \overline{i^2_{DS4B}} + \left(\frac{g_{m9B}}{g_{m8B}}\right)^2 \overline{i^2_{DS8B}} \tag{39}$$

$$\overline{V_Z^2} \cong 4kT\gamma R_{MOS} + \frac{KF}{2C_{OX}WLK'}\frac{1}{f} \tag{40}$$

Substituting the equations from Equation 32 yields the equivalent input referred voltage noise for the 2nd order low pass filter.

$$\overline{V^2_{IRN(2^{nd})}} \cong 2\left[\begin{array}{c} \frac{\overline{i^2_{D1}} + \overline{i^2_{D2}} + \overline{i^2_{D5}} + \overline{i^2_{D6}}}{g^2_{m1}} + \cdots \\ \left(4kT\gamma R_{MOS} + \frac{KF}{2C_{OX}WLK'}\frac{1}{f}\right) + \cdots \\ 4R_1^2\left(\overline{i^2_{DS8C}} + \overline{i^2_{DS2D}} + \left(\frac{g_{m2D}}{g_{m1D}}\right)^2 \overline{i^2_{DS1D}} + \left(\frac{g_{m8C}}{g_{m6C}}\right)^2 \left(\overline{i^2_{DS5C}} + \overline{i^2_{DS6C}} + \overline{i^2_{DS9}} + \overline{i^2_{DS10}}\right)\right) + \cdots \\ R_1^2\left(\overline{i^2_{DS5B}} + \overline{i^2_{DS9B}} + \left(\frac{g_{m5B}}{g_{m4B}}\right)^2 \overline{i^2_{DS4B}} + \left(\frac{g_{m9B}}{g_{m8B}}\right)^2 \overline{i^2_{DS8B}}\right) \end{array}\right] \tag{41}$$

Equation 41 shows that some filter parameters inversely affect noise, while others increase it. Table 4 presents how input referred voltage noise varies with these parameters. It's

Table 4 Noise analysis of the applied filter for various parameters

Parameters	Input Referred Voltage Noise	fCUT	dB Loss	Parameters	Input Referred Voltage Noise	fCUT	dB Loss
RMOS	19.98mV	29.3 kHz	-1 dB	$\frac{RMOS}{\sqrt{2}}$	14.15mV	41.1 kHz	-1 dB
$g_{m1,2}$	19.98mV	29.3 kHz	-1 dB	$\frac{gm1,2}{\sqrt{2}}$	20.37mV	30 kHz	-1 dB
$g_{m5C,6C}$	19.98mV	29.3 kHz	-1 dB	$\frac{gm5C,6C}{\sqrt{2}}$	39.75mV	16.4 kHz	-1.6 dB
$g_{m1D,2D}$	19.98mV	29.3 kHz	-1 dB	$\frac{gm1D,2D}{\sqrt{2}}$	26.49mV	22.8 kHz	-1.2 dB
$g_{m9,10}$	19.98mV	29.3 kHz	-1 dB	$\frac{gm9,10}{\sqrt{2}}$	16.17mV	35.9 kHz	-1 dB

*The gm values were altered by changing the channel lengths (L) of the transistors.

also crucial to maintain the filter's characteristic properties during these variations.

The table confirms the equivalent input referred voltage noise for the 2nd order low pass filter, showing that changes in parameter values affect noise levels. Table 4 indicates that reducing noise by 19% can shift the cut-off frequency by 22% at the optimal configuration (gm9,10). Depending on application needs, one can select the best configuration or explore alternatives by adjusting other parameters

CONCLUSION

In this study explores noise analysis and optimization for filters using two active element based capacitor multiplier structures: MO-VDTA and MO-CDTA. Both structures offer an adjustable multiplication factor "k", allowing operation across various cutoff frequencies for different applications. The MO-VDTA structure provides a multiplication factor ranging from 120 to 750, with a filter cutoff frequency from 2 kHz to 12.4 kHz. Initial input referred noise is 10.13 mV, reduced to 6.19 mV (40% decrease) through optimization, even though this causes a 20% variation in cutoff frequency. For the MO-CDTA structure, the multiplication factor also ranges from 120 to 750, with cutoff frequencies between 400 Hz and 1250 Hz. Initial input referred noise is 19.98 mV, reduced to 16.17 mV (19% decrease), resulting in a 22% change in cutoff frequency. In the noise analyses of filters, additional parasitic effects of the active elements were not included in the calculations to facilitate easier interpretation of the equations. Additionally, only the transistors with dominant noise contributions were considered. The findings highlight the need for noise optimization in low frequency applications and provide mathematical expressions for factors affecting noise. The results demonstrate that while reducing noise can decrease the cut off frequency, the trade-offs between noise and cut off frequency vary with application. Future research will investigate additional noise parameters for the further performance optimization.

Acknowledgment

The author received no financial support for the research, authorship, and/or publication of this article.

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