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A Hybrid Non-isolated DC-DC Power Electronic Conversion Topology with High Step-up Gain and Low Switch Voltage Stress

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Highlights

- Improved voltage gain is achieved using hybrid converter topology.
- Both SEPIC and modified Cuk converters in hybrid structure are operated at same duty cycle.
- The proposed hybrid topology employs lower passive component-count.
- A prototype model of the projected converter validates its performance.

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Integrated SEPIC-Modified cuk topology, Prototype model, Steady state performance, Voltage gain, Voltage stress

Abstract

The renewable energy based electrical power generation has the natural characteristics such as unpredictability and intermittency. The challenging task is continuous power supply that is obtained by hybrid system consisting of two or more resources. This research article proposes a transformer-less integrated DC-DC conversion scheme, composed of parallel-connected modified Cuk and conventional Single-Ended-Primary-Inductor Converter (SEPIC) topologies, suitable for application in power generation using renewable sources. The suggested integrated converter topology is operated in such condition that inductor current is continuous, and it employs lower passive component-count and provides a higher voltage conversion ratio than the traditional non-isolated configurations. The power semiconductor devices experience low voltage stress. The steady state performance of the proposed hybrid topology along with the mathematical derivation of voltage gain is explored. A prototype model of the converter is implemented to validate the performance of the hybrid configuration. The output voltage and other performance parameters of the hardware model are compared with that of the simulink setup.

1. INTRODUCTION

The large amount of electrical energy demanded by commercial and industrial consumers globally can be met out by both traditional and renewable sources of energy. Even though the efficiency of non-renewable fossil fuel based energy generation is high, such method of power generation includes certain disadvantages like global environment pollution and sudden rise of earth's surface temperature. Moreover, the non-renewable energy sources have limited availability, and are depleting day by day as the population growth increases in India [1]. Hence, the alternate method of electrical power generation using renewable energy sources is chosen [2, 3]. The renewable sources like solar panels can produce low level DC output only [4]. The low DC voltage of solar sources is not sufficient to drive the inverters connected to the grid. Hence, DC-DC power electronic converters capable of producing higher output voltages are used as interface between renewable sources and inverters. The researchers concentrate on the development of both transformer-less and isolated structures of DC-DC conversion schemes suitable for various applications [5-15]. There are certain advantages and disadvantages associated with each of the structures [16]. The selection of appropriate converter topology is influenced by specific application requirements [17, 18].

A transformer-less modified single power switch configured SEPIC topology, with relatively improved voltage conversion ratio and converter efficiency compared to that with traditional boost, SEPIC, and modified SEPIC structures, is proposed in [19], where the input current requirement and switch voltage

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stress are low. A hardware structure of highly efficient modified single-switch configured SEPIC topology with additional passive components was developed by some authors for obtaining improved voltage gain by means of turn's ratio adjustment of coupled inductor [20]. A broad range of voltage conversion ratio, that is reconfigurable as per demand on input side, can be achieved using a high reliability DC-DC converter structure composed of conventional SEPIC converter with 'n' number of extended units [21]. Some authors suggested the magnetic coupling based voltage gain improvement for the modified high efficiency SEPIC structures which find applications in renewable energy based power generation [22]. A modified high voltage gain SEPIC configuration with single controlled switch is proposed in [23] for DC microgrid applications. The voltage gain improvement by a modified SEPIC topology composed of a traditional SEPIC structure combined with a voltage multiplier cell can be achieved at low duty cycle itself based on integrated inductor scheme [24].

A new non-isolated CUK topology with reduced switch voltage stress, composed of a modified CUK configuration and n-number of voltage multiplier units, is proposed by some authors in view of achieving high voltage gain at low duty cycle itself [25]. A modified configuration of interleaved Cuk converter, that can provide enhanced voltage gain and reduced ripples in the output voltage, is presented in [26]. A transformer-less DC-DC power electronic converter based on Cuk configuration is developed to produce both enhanced voltage conversion ratio and power conversion efficiency using voltage-lift technique [27]. A simple structure of a high efficiency bi-directional Cuk topology with optimized turn ratio of tapped inductor, capable of having high voltage conversion ratio in both step-up and step-down modes, is proposed in [28]. The drawback of the converter proposed in [28] is that one switch has low voltage stress and another switch has high voltage stress. A reduced size arrangement of traditional Cuk topology without adding any passive elements can have enhanced efficiency with reduced device currents by means of a lower voltage rated coupling capacitor of smaller size [29].

An improved voltage gain can be produced using non-isolated hybrid converter configuration suggested by the author in [30], where the integrated structure is composed of a traditional boost and modified Cuk topologies. The work proposed in [30] explores the steady state operational behavior and dynamic modeling of the integrated converter structure. Some authors proposed a transformer-less single power switch based Zeta-Mahafzah topologies combined DC-DC power conversion scheme, capable of providing higher output voltages at low duty cycle ratio itself and synchronized multiple DC outputs required for certain applications [31]. Moreover, the converter proposed in [31] exhibits improved steady state behavior and reliability, and the semiconductor devices are subjected to lower voltage stress. An another integrated single power switch based DC-DC power electronic converter comprising Luo as well as flyback converters with voltage multiplier circuit for boosting the voltage level is proposed by some authors for renewable energy sources based power generation [32]. In comparison with the conventional boost, SEPIC, and Cuk structures, the projected configuration in [32] has the advantages such as enhanced efficiency and voltage conversion ratio due to coupled-inductor concept, low ripple present in input current, lower voltage stress of semiconductor based components, and lower conduction as well as switching losses.

Some authors developed a highly efficient non-isolated single switch category of hybrid reduced component-count DC-DC converter, composed of traditional boost and Cuk structures, to yield enhanced voltage conversion ratio [33]. The enhancement of voltage gain and power density is obtained by a DC-DC converter structure, composed of magnetic integrated switching inductor based single-switch boost-Cuk topologies, in which the input and output currents are continuous with minimum ripples [34]. A solar powered integrated single-switch structure of CUK-SEPIC configurations is capable to achieve (i). enhanced voltage conversion ratio when the duty cycle ratio is increased above 0.5, and (ii). high step-down voltage conversion ratio with duty cycle ratio less than 0.5 respectively [35]. The inductor magnetic coupling on the input as well as output sides in the converter structure projected in [35] ensures lower amount of current ripples that can facilitate the maximum extraction of solar power through MPPT technique. A transformer-less single-switch configured hybrid DC-DC conversion scheme comprising the traditional SEPIC and CUK structures, capable of providing improved voltage conversion ratio, is proposed in [36], where the Fractional Order PID (FOPID) controller is employed to improve the converter's dynamic behavior.

The research work proposed in this article presents the theoretical steady state behavior and experimental verification of a transformer-less integrated SEPIC and modified Cuk based DC-DC power electronic converter. The projected converter has relatively enhanced voltage conversion ratio compared to that with conventional SEPIC and Cuk topologies. The operation of suggested converter is such that the inductors carry current continuously. The semiconductor based components employed in the converter experience reduced voltage stress.

The proposed research work consists of various sections. The converter operation during steady state is presented in the following section. The MATLAB/SIMULINK tool based simulation and prototype model results are discussed in subsequent section for the suggested converter. Finally, the conclusion part highlights the key points of the work presented in this article.

2. THE SUGGESTED TRANSFORMER-LESS SEPIC-MODIFIED CUK COMBINED DC-DC CONVERTER CONFIGURATION

The research article presented here explores the steady state continuous conduction mode behavior and prototype model analysis of a transformer-less SEPIC-modified Cuk combined DC-DC power electronic converter topology capable of providing enhanced step-up gain at low duty factor (k). The working and the derivation of voltage gain expression for the converter are discussed in the following paragraphs.

2.1. Operating Principle of the Suggested Converter Topology

The structure of the proposed transformer-less integrated DC-DC converter comprising modified Cuk and SEPIC topologies is shown in Figure 1, in which the combination of 'Boost portion' and 'Cuk converter' constitutes the modified Cuk configuration. It consists of two input DC sources V_{in}, semiconductor based components such as power switches (MOSFET switches S_1 and S_2) and uncontrolled components (D_1, D_2, D_3, and D_4), four continuously current carrying inductors L_1, L_2, L_3, and L_0, four capacitors C_1, C_2, C_3, and C_0, and a resistive load R_0. The converter analysis starts with certain assumptions: (i). All the inductors are very large and the currents in them are constant. (ii). All the capacitors are very large and the voltages across them are constant. (iii). The steady state operation of the converter circuit is considered. (iv). The power switch with duty ratio k is triggered by a PWM signal of time period T and the switch is closed for time kT and opened for time (1-k)T. (v). All the active and passive components are assumed to be ideal. (vi). The proposed converter circuit is operated in continuous conduction mode. The projected integrated structure exhibits improved voltage gain at low duty cycle itself by complementing the positive features of both modified Cuk and SEPIC configurations. Moreover, the reduced voltage stress is observed on the power switches and the diodes. The suggested converter is operated in four different modes as explained below:

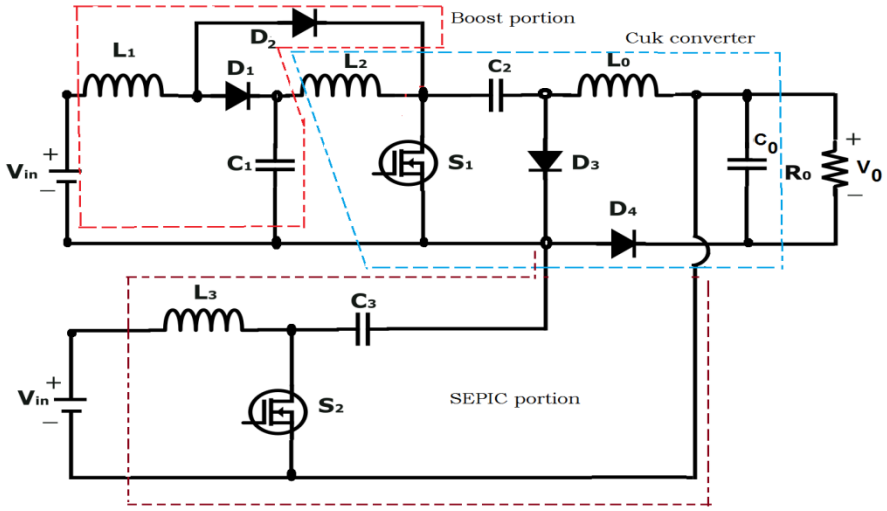


Figure 1. *Proposed non-isolated integrated modified Cuk-SEPIC topology*

The circuit topology of the converter during Mode-I is illustrated in Figure 2. The power MOSFET switches (S_1 and S_2) are allowed to conduct by the pulse width modulated (PWM) signals. The uncontrolled semiconductor components such as D_1, D_3, and D_4 are acting as open circuit due to reverse bias condition, and the diode D_2 acts as short circuit due to forward bias. The supply voltage V_{in} charges the inductors L_1 and L_3. The capacitors C_1 charges the inductor L_2. The capacitors C_2 and C_3 discharge to charge the inductor L_0. The voltages across the four identical inductors are written as shown below (Equation (1)):

$$V_{L1} = V_{in}\,; \qquad V_{L2} = V_{C1}\,; \qquad V_{L3} = V_{in}\,; \qquad V_{L0} = V_{C2} + V_{C3}\,. \tag{1}$$

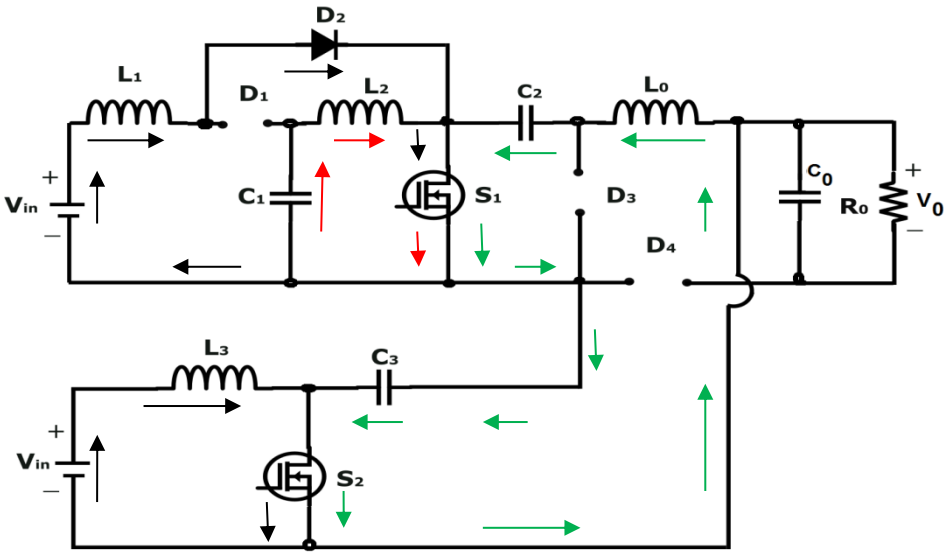


Figure 2. *Converter circuit configuration during Mode-I*

The converter operation during Mode-II is explained using the circuit configuration shown in Figure 3, where the MOSFET switch S_1 continues to conduct and the MOSFET switch S_2 is now allowed to act as open circuit. The uncontrolled semiconductor devices D_2 and D_4 are now allowed to act as short circuit due to forward bias, and the devices D_1 and D_3 are open circuited due to reverse bias situation. The capacitor C_1 delivers the stored energy and hence charges the inductor L_2. The capacitor C_0 gets charged by C_2 as shown in Figure 3. The voltages across the four identical inductors are written as shown below (Equation (2)):

$$V_{L1} = V_{in}\,; \qquad V_{L2} = V_{C1}\,; \qquad V_{L3} = V_{in} - V_{C3} - V_0\,; \qquad V_{L0} = V_{C2} - V_0\,. \tag{2}$$

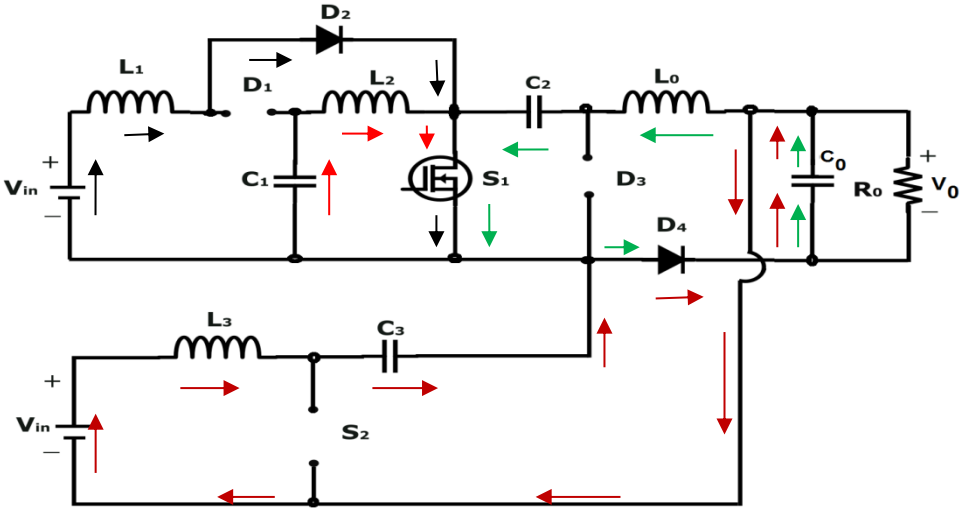


Figure 3. *Converter circuit configuration during Mode-II*

The working of the converter under Mode-III is illustrated by the circuit topology shown in Figure 4, where the MOSFET switch S_1 is allowed to act as open circuit and the MOSFET switch S_2 is now triggered into conduction by applying a PWM signal. The uncontrolled semiconductor devices D_1 and D_3 are allowed to conduct, and the devices D_2 and D_4 are prevented from conduction. The capacitor C_1 is charged by discharge of L_1. The inductor L_2 discharges through C_2, D_3, and C_1. The capacitor C_3 gets charged by discharge of L_0. The voltages of the four identical inductors are expressed as shown below (Equation (3)):

$$V_{L1} = V_{in} - V_{C1}\,; \qquad V_{L2} = V_{C1} - V_{C2}\,; \qquad V_{L3} = V_{in}\,; \qquad V_{L0} = V_{C3}\,. \tag{3}$$

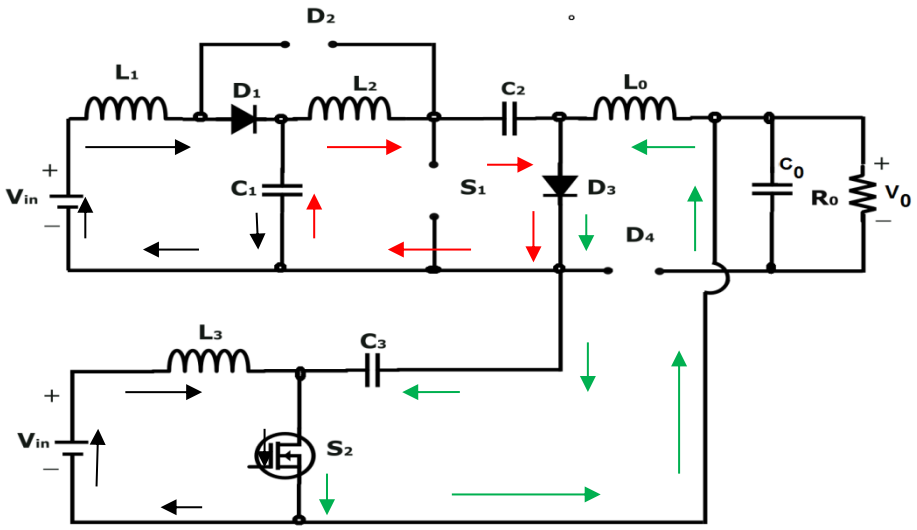


Figure 4. *Converter circuit configuration during Mode-III*

In Mode-IV as illustrated by the circuit configuration in Figure 5, both the MOSFET switches are now allowed to act as open circuited path. The diodes D_1, D_3 and D_4 act as short-circuited path due to forward bias situation. The reverse bias situation of the device D_2 is continued. The inductor L_1 delivers the stored energy, thereby charging the capacitor C_1. The inductor L_2 discharges through the diode D_3, thereby charging the capacitor C_2. At the same time, the inductor L_0 discharges through the capacitor C_0 to charge it. The potential differences across the four identical inductors are expressed as shown below (Equation (4)):

$$V_{L1} = V_{in} - V_{C1}\,; \qquad V_{L2} = V_{C1} - V_{C2}\,; \qquad V_{L3} = V_{in} - V_{C3} - V_0\,; \qquad V_{L0} = -V_0\,. \tag{4}$$

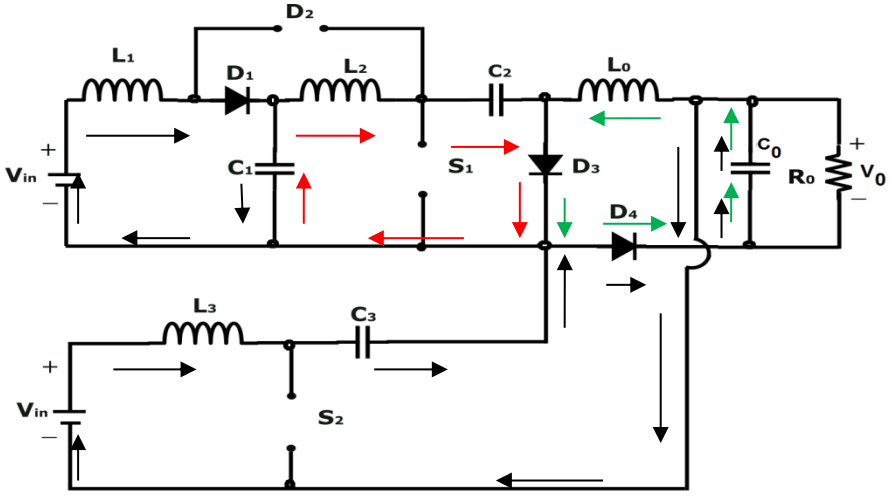
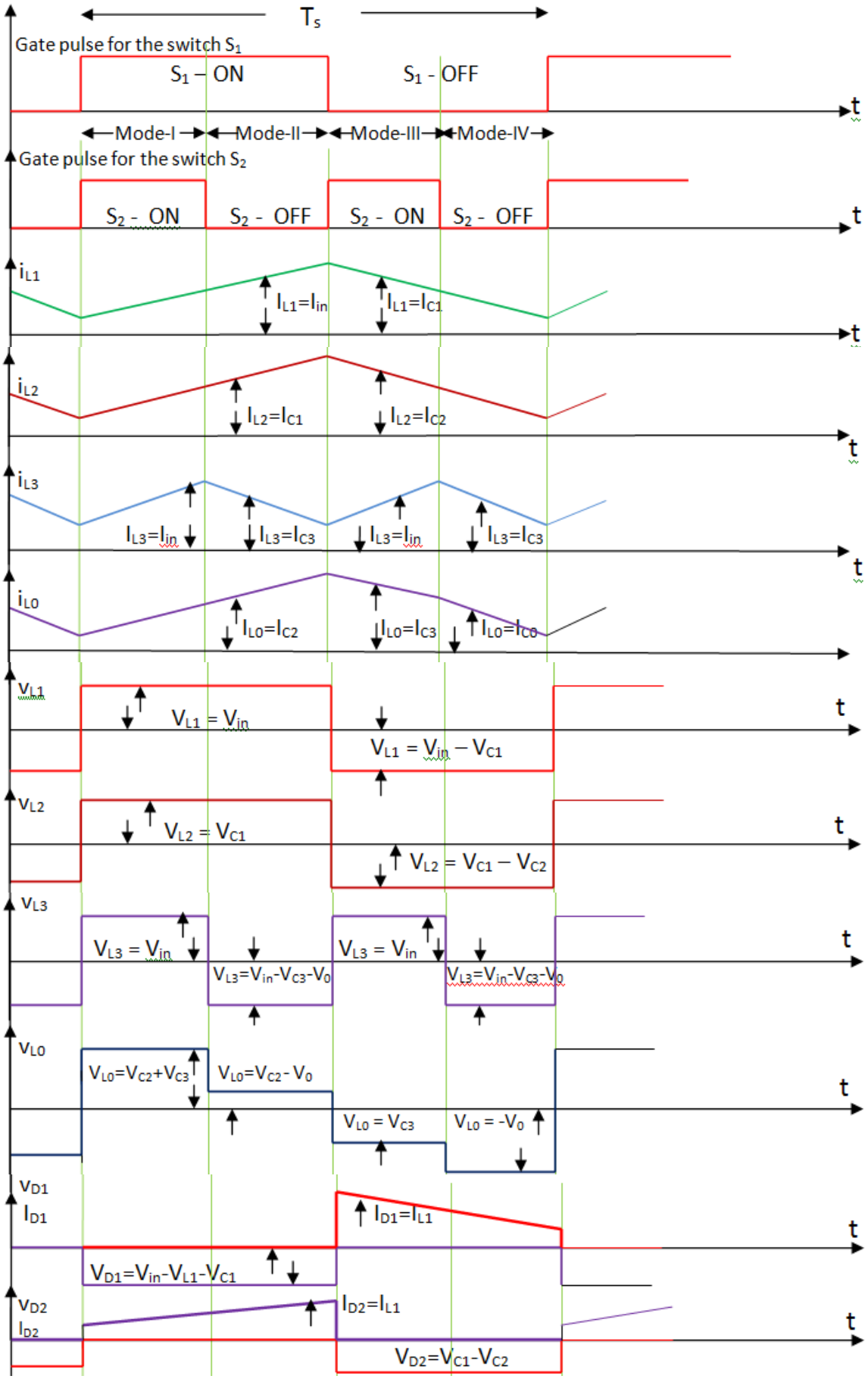


Figure 5. *Converter circuit configuration during Mode-IV*

The key waveforms of the proposed converter are shown in Figure 6.


Ts
Gate pulse for the switch S1
S1 – ON
S1 - OFF
t
Mode-I
Mode-II
Mode-III
Mode-IV
Gate pulse for the switch S2
S2 - ON
S2 - OFF
S2 - ON
S2 - OFF
iL1
IL1=Iin
IL1=IC1
iL2
IL2=IC1
IL2=IC2
iL3
IL3=Iin
IL3=IC3
IL3=Iin
IL3=IC3
iL0
IL0=IC2
IL0=IC3
IL0=IC0
VL1
VL1 = Vin
VL1 = Vin – VC1
VL2
VL2 = VC1
VL2 = VC1 – VC2
VL3
VL3 = Vin
VL3=Vin-VC3-V0
VL3 = Vin
VL3=Vin-VC3-V0
VL0
VL0=VC2+VC3
VL0=VC2- V0
VL0 = VC3
VL0 = -V0
VD1
ID1
ID1=IL1
VD1=Vin-VL1-VC1
VD2
ID2
ID2=IL1
VD2=VC1-VC2

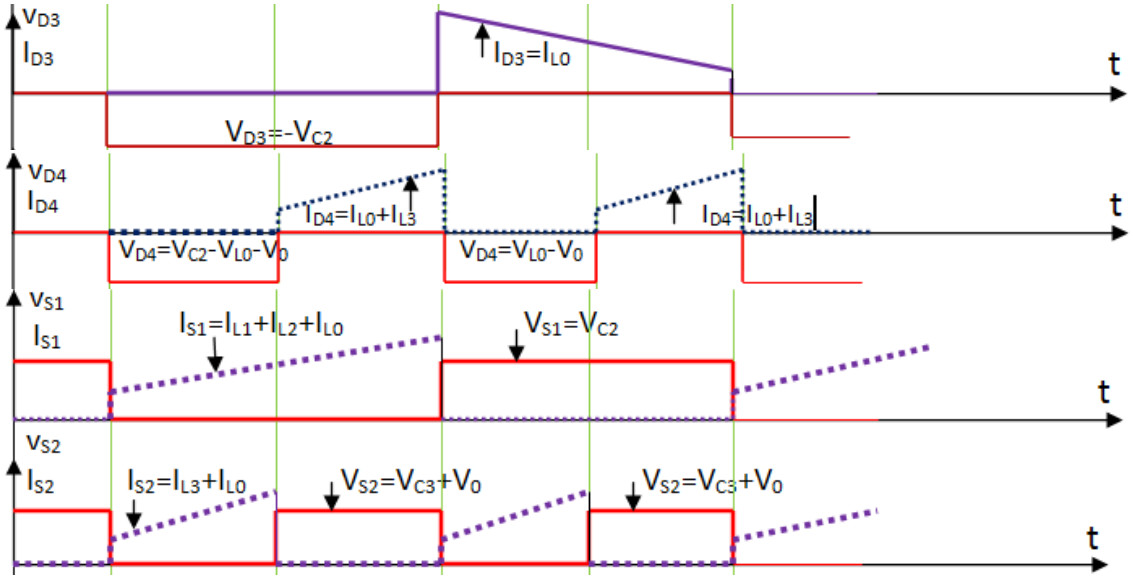


Figure 6. *Key waveforms of the proposed converter*

2.2. Voltage Gain Derivation and Active Switch Stress Analysis for the Projected Integrated DC-DC Converter Topology

The Equations (1) to (4) are used to obtain an expression for the voltage gain (G) of the suggested integrated converter configuration. The application of volt-second balance approach for the four inductors during the various converter modes yields the Equations (5), (7), (9), and (11) respectively.

$$V_{in}kT_s + (1-k)(V_{in} - V_{C1})T_s = 0. \tag{5}$$

The capacitor voltage (V_{C1}) is given by Equation (6).

$$V_{C1} = \frac{V_{in}}{(1-k)} \tag{6}$$

$$V_{C1}kT_s + (1-k)(V_{C1} - V_{C2})T_s = 0. \tag{7}$$

The capacitor voltage (V_{C2}) is obtained as Equation (8).

$$V_{C2} = \frac{V_{in}}{(1-k)^2} \tag{8}$$

$$V_{in}kT_s + (1-k)(V_{in} - V_{C3} - V_0)T_s = 0. \tag{9}$$

The capacitor voltage (V_{C3}) is given by Equation (10).

$$V_{C3} = \frac{V_{in}}{(1-k)} - V_0 \tag{10}$$

$$(V_{C2} + V_{C3})kT_s - V_0(1-k)T_s = 0, \tag{11}$$

where, V_{in} - Input DC voltage (V); k – Duty factor of the converter; V_0 - Output DC voltage (V); T_s - Switching period (s).

By substituting the Equations (8) and (10) in Equation (11), the voltage gain (G) of the projected converter is obtained as Equation (12).

$$G = \frac{V_0}{V_{in}} = \frac{k}{(1-k)}\left(\frac{1}{(1-k)} + 1\right). \quad (12)$$

The Equation (12) clearly indicates that the voltage gain of the projected converter has higher value for the given duty factor (k), compared with that of conventional CUK and SEPIC topologies [6] as shown in Figure 7. As the conventional CUK and SEPIC topologies have the same absolute values of voltage gains as illustrated by the Equations (13) and (14), the voltage gain curves of both the topologies merge as shown in Figure 7. Table 1 illustrates the active switch voltage and current stress comparison of the proposed converter with that of the conventional single-switch SEPIC and CUK topologies.

Voltage gain (G) for the traditional SEPIC topology = $G = \frac{k}{(1-k)}$ (13)

Absolute Voltage gain (G) for the traditional Cuk converter = $|G| = \frac{k}{(1-k)}$ (14)

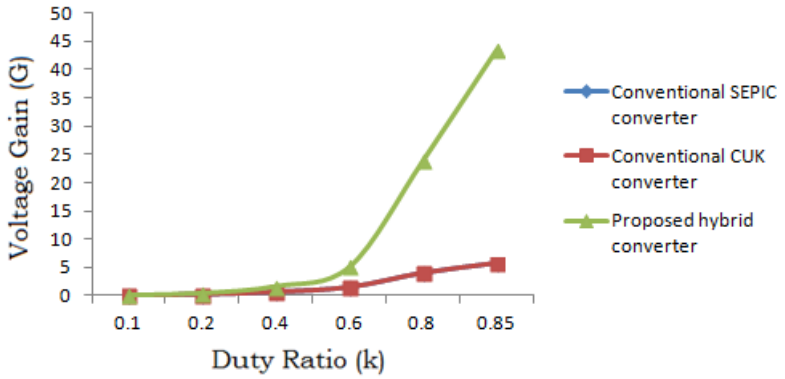


Figure 7. *Voltage gain comparison of converters*

Table 1*. Active switch voltage and current stress comparison of converters*

Converters	Voltage stress across the active switch (V)	Current stress of the active switch (A)
Conventional single-switch SEPIC topology [6]	$V_S = \frac{V_{in}}{(1-k)}$	$I_S = I_{L1} + I_{L2}$
Conventional single-switch CUK topology [6]	$V_S = \frac{V_{in}}{(1-k)}$	$I_S = I_{L1} + I_{L2}$
Proposed converter	$V_{S1} = V_{C2} = \frac{V_{in}}{(1-k)^2}$	$I_{S1} = I_{L1} + I_{L2} + I_{L0}$
	$V_{S2} = V_{C3} + V_0 = \frac{V_{in}}{(1-k)}$	$I_{S2} = I_{L3} + I_{L0}$

3. SIMULATION AND HARDWARE RESULTS FOR THE PROJECTED CONVERTER

The theoretical steady state behavior of the proposed integrated converter structure is validated using both (i). Simulation platform, and (ii). Prototype model. The results are presented for both cases.

3.1. Converter Model Using MATLAB / SIMULINK Tool and its Results

The MATLAB/SIMULINK model of the continuous conduction mode operation of the suggested converter is developed and is simulated to validate its performance. The simulink model of the topology is illustrated

in Figure 8. The converter switching frequency (f_s) of 15 kHz is set in the simulation. The passive elements are designed as per the specifications [36]. A pure resistor of 300 Ω is used as load (R_0) across the converter output terminals. The various simulation parameters of the converter are listed in Table 2. The Pulse Width Modulated signals shown in Figure 9 are used to turn ON the power switches S_1 and S_2. The traditional SEPIC and modified Cuk structures are energized separately by a DC source (V_{in}) of 12 V magnitude, as shown in Figure 10. The resulting source currents (I_{in}) of the converters are depicted in Figures 11 and 12 respectively. The load voltage (V_0) of nearly 61.6 V and the load current (I_0) of around 0.98 A are obtained for the projected hybrid topology with the chosen duty cycle ratio k = 0.6 for each of the MOSFET switches S_1 and S_2 to simplify the analysis, as illustrated in Figures 13 and 14 respectively. During the operation of the converter, the semiconductor based components experience low potential stress during reverse bias condition. The switches S_1 and S_2 experience peak voltage stresses (V_{S1} and V_{S2}) of around 76.5 V and 39 V respectively as shown in Figures 15 and 16 respectively. Another set of above waveforms is taken by considering the input voltage V_{in} as 24 V and the duty ratio k as 0.7, and the corresponding waveforms are shown in Figures from Figures 17-25, respectively. The voltage stress comparison of similar converter structures is given in Table 3. The steady state behavior of the topology is analyzed by choosing the duty factor (k) for the power switches in the range from 0.5 to 0.9.

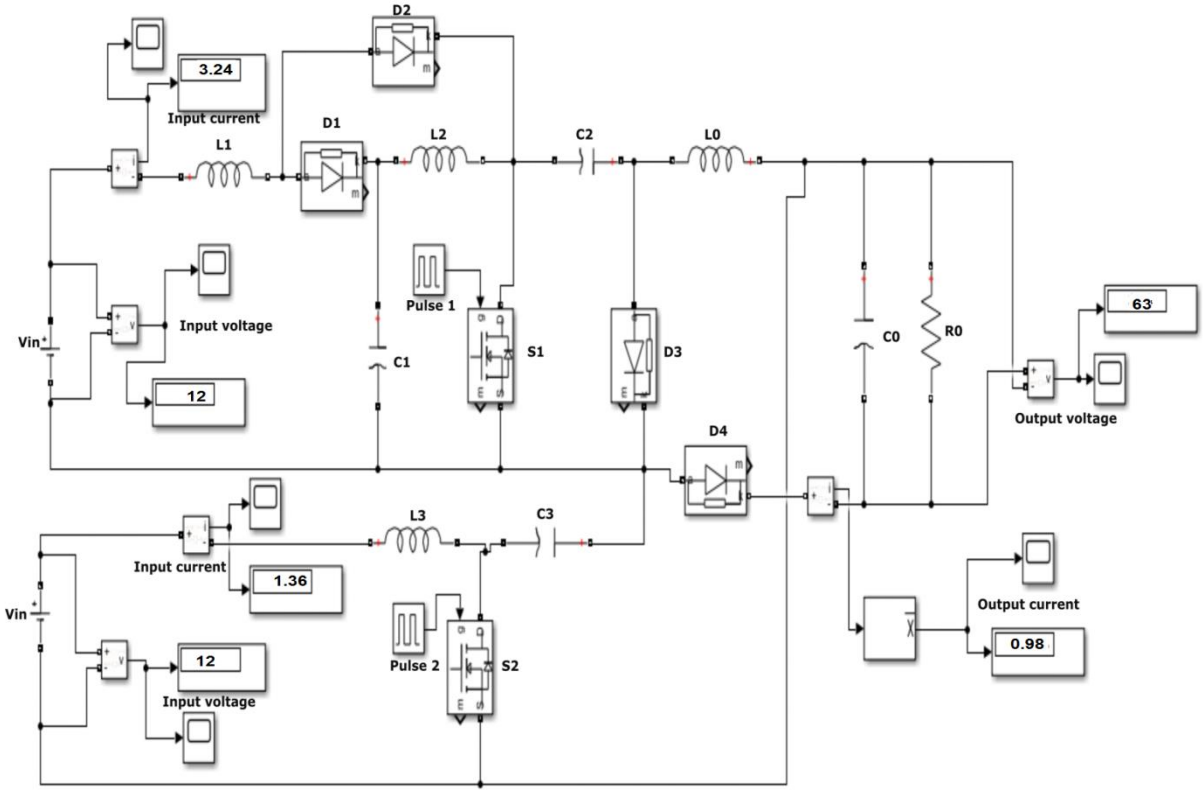


Figure 8. *Proposed converter model using MATLAB / SIMULINK tool*

Table 2*. Converter simulation parameters*

Parameters	Symbol	Value
DC input voltage to each converter	V_{in}	12 V
Inductors	L_1, L_2, L_3, L_0	700 µH each
Capacitor	C_1	100 µF
Capacitors	C_2, C_3	3.3 µF each
Capacitor	C_0	1000 µF
Load resistor	R_0	300 Ω
Switching frequency	f_s	15 kHz
Duty factor (k) of the switches S_1 & S_2	k	0.6 each

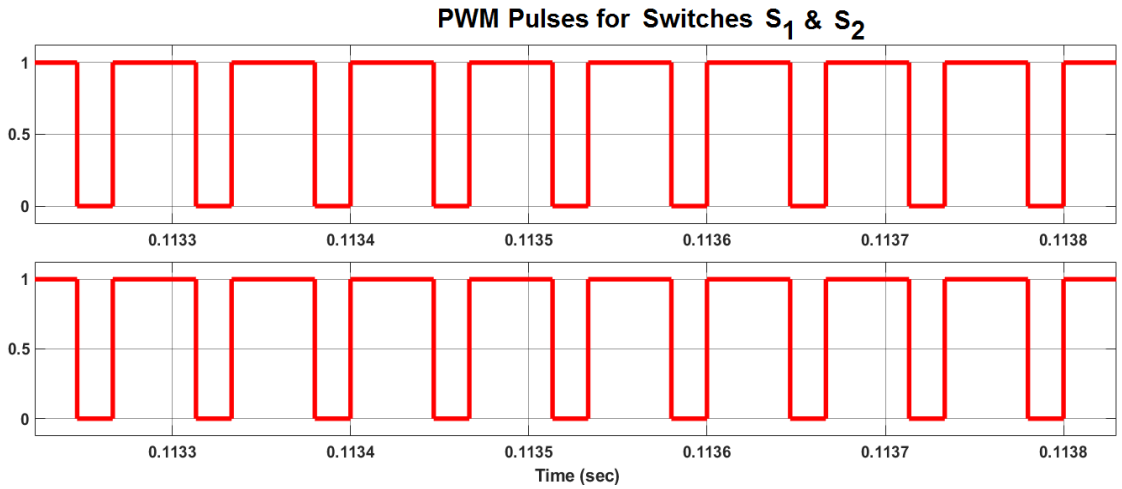


Figure 9. *PWM signals for triggering the power switches*

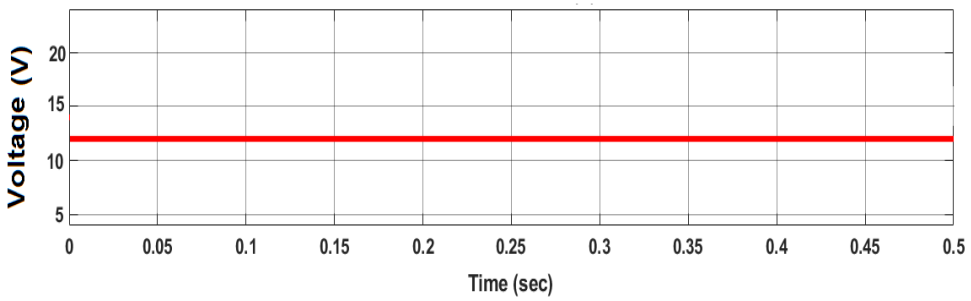


Figure 10. *12V DC input voltage (V_{in}) to both Modified Cuk converter and SEPIC structure*

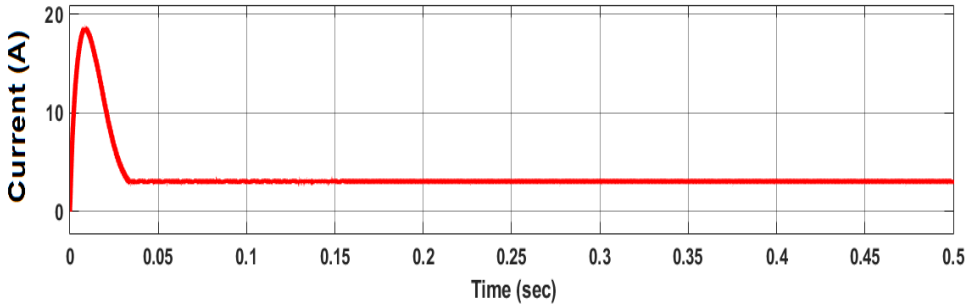


Figure 11. *DC input current (I_{in}) to Modified Cuk converter with V_{in} = 12 V*

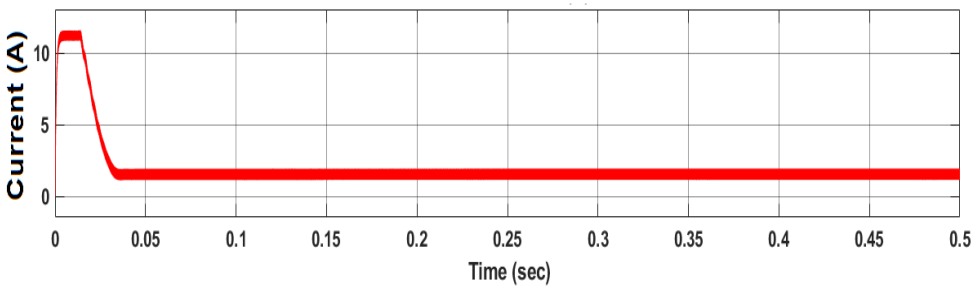


Figure 12. *DC input current (I_{in}) to SEPIC structure with V_{in} = 12 V*

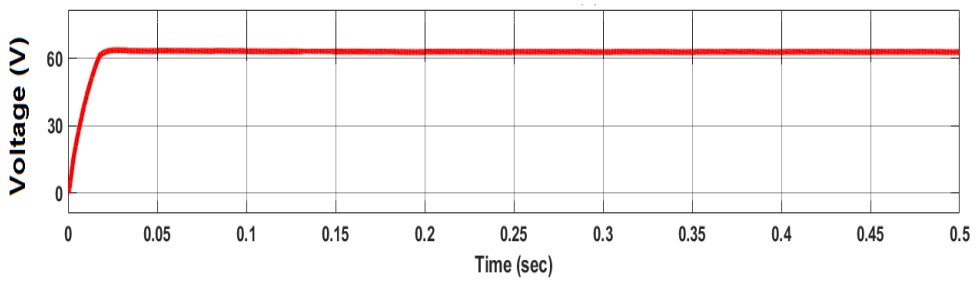


Figure 13. *Output voltage (V_0) of integrated converter structure with V_{in} = 12 V*

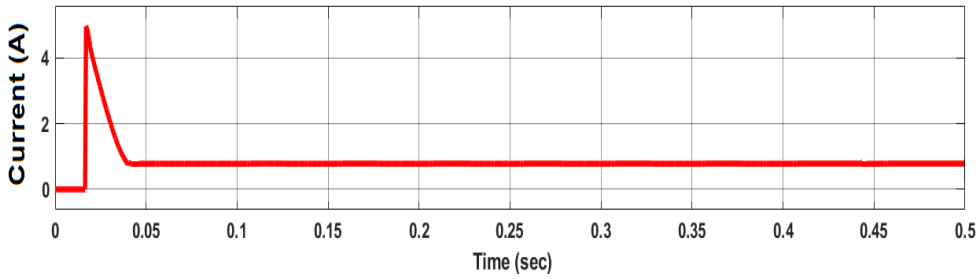


Figure 14. *Output current (I_0) of integrated converter structure with V_{in} = 12 V*

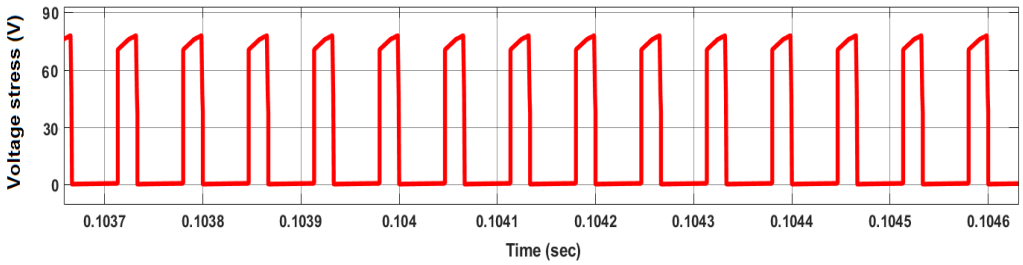


Figure 15. *Voltage stress (V_{S1}) of MOSFET switch S_1 with V_{in} = 12 V*

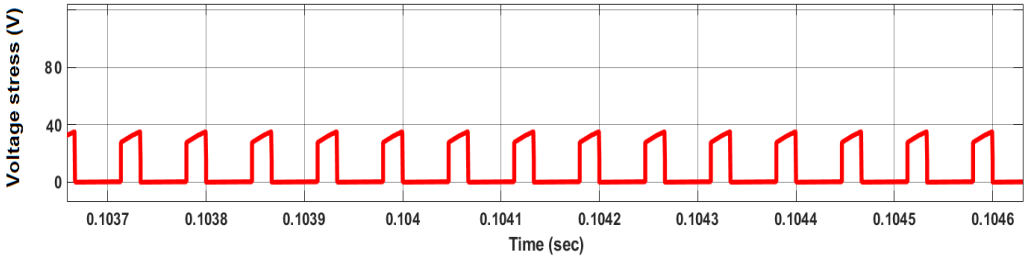


Figure 16. *Voltage stress (V_{S2}) of MOSFET switch S_2 with V_{in} = 12 V*

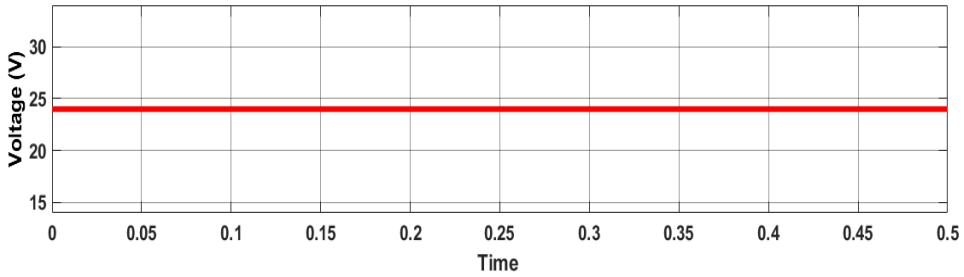


Figure 17. *24V DC input voltage (V_{in}) to both Modified Cuk converter and SEPIC structure*

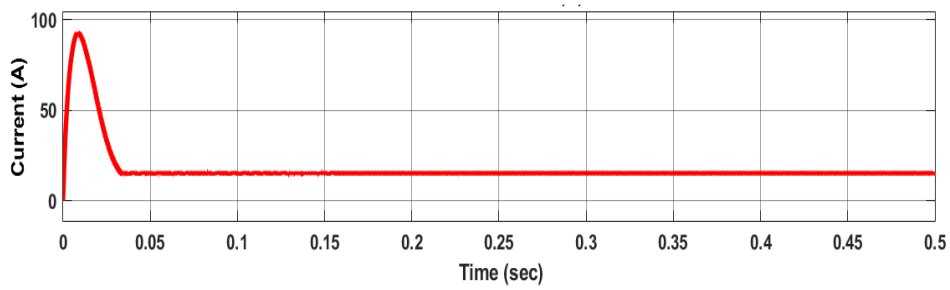


Figure 18. *DC input current (I_{in}) to Modified Cuk converter with V_{in} = 24 V & k = 0.7*

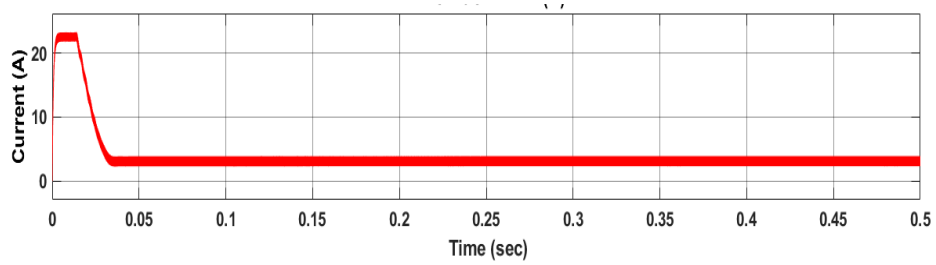


Figure 19. *DC input current (I_{in}) to SEPIC structure with V_{in} = 24 V & k = 0.7*

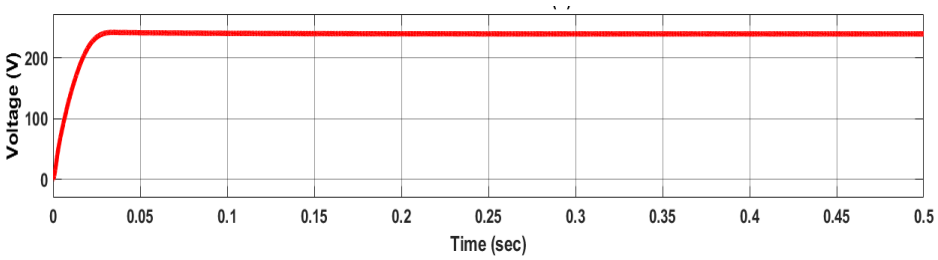


Figure 20. *Output voltage (V_0) of integrated converter structure with V_{in} = 24 V & k = 0.7*

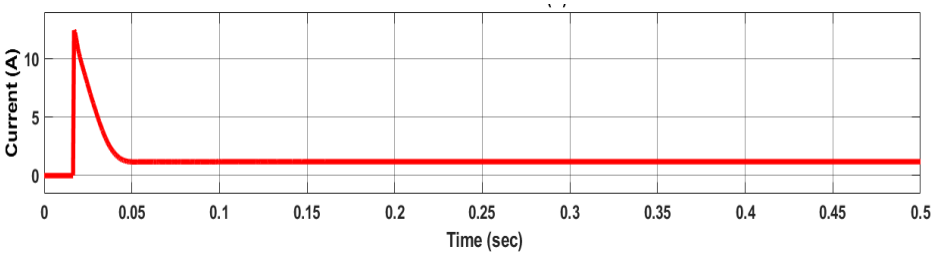


Figure 21. *Output current (I_0) of integrated converter structure with V_{in} = 24 V & k = 0.7*

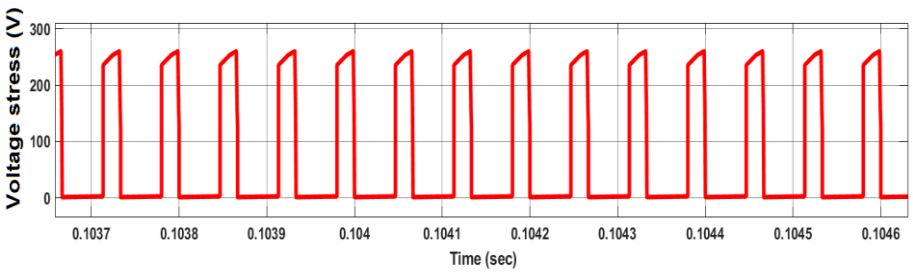


Figure 22. *Voltage stress (V_{S1}) of MOSFET switch S_1 with V_{in} = 24 V & k = 0.7*

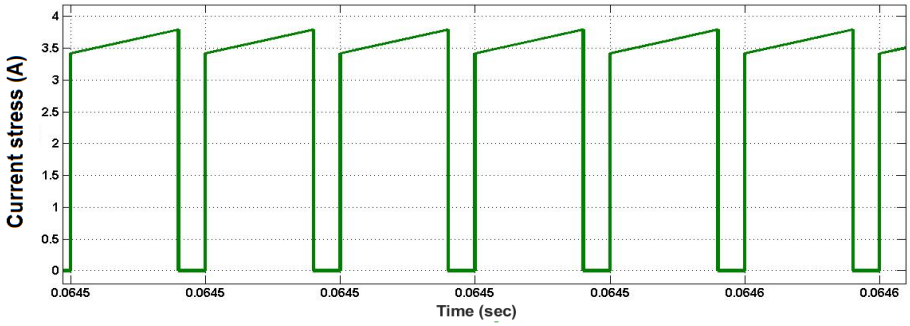


Figure 23. *Current stress (I_{S1}) of MOSFET switch S_1 with V_{in} = 24 V & k = 0.7*

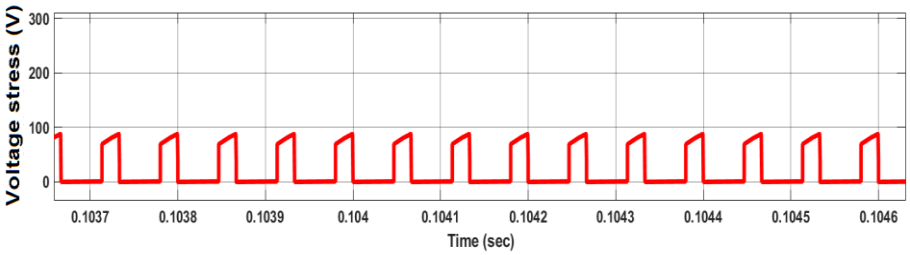


Figure 24. *Voltage stress (V_{S2}) of MOSFET switch S_2 with V_{in} = 24 V & k = 0.7*

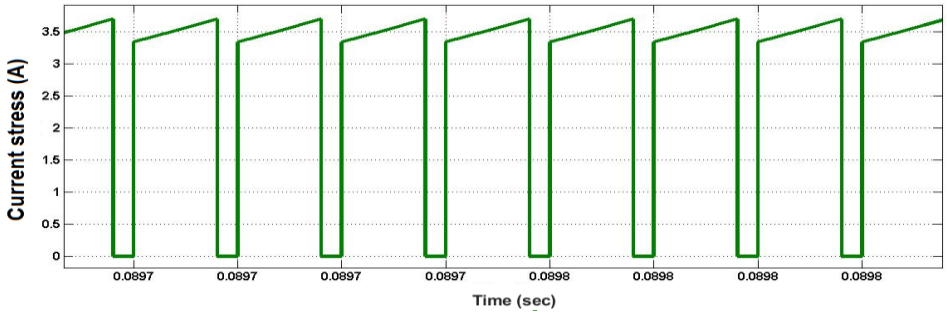


Figure 25. *Current stress (I_{S2}) of MOSFET switch S_2 with V_{in} = 24 V & k = 0.7*

Table 3*. Active switch voltage stress comparison of similar converter structures*

Converter structures	Voltage stress on the active switch
Converter [33]	High
Converter [30]	Less
Converter [36]	Less
Converter [34]	High
Converter [32]	Less
Proposed Converter	Moderate for both switches

3.2. Prototype Converter Model and its Results

The simulation results of the projected hybrid converter topology are validated through experimental results obtained using hardware setup as illustrated in Figure 26. Table 4 lists the specifications of components and parameters employed in the hardware configuration. The dsPIC30F2010 microcontroller unit is not capable enough to charge the gate capacitance of a power MOSFET as it produces a low power output signal. Hence, a TLP250H MOSFET gate driver circuit is used as an interface between the controller and the MOSFET switch. The gate driver circuit accepts the controller output and produces appropriate high current gate pulses of 60% duty cycle for both controlled switches as illustrated in Figure 27. The prototype model is switched at a frequency (f_s) of 15 kHz. There are two DC sources (V_{in}) employed in the hardware arrangement to energize separately the SEPIC and modified Cuk structures; (i). A battery of 12 V with 7.5 Ah capacity, and (ii). A 12 V regulated power supply unit. The corresponding practical waveforms of source voltage (V_{in}) and source current (I_{in}) are depicted separately in Figures 28 and 29 respectively for both the

SEPIC and modified Cuk topologies. Figure 30 illustrates that the projected integrated DC-DC converter configuration with 60% duty cycle can produce an output voltage (V_0) of 60.2 V and an output current (I_0) of 0.965 A when supplying power to a 60 W lamp load. The maximum switch voltage stresses are measured as 76 V and 38.4 V for both controlled switches respectively, as depicted in Figures 31 and 32, respectively. A DSO (Digital Storage Oscilloscope) is employed to display all the waveforms. Table 5 shows the comparison of simulation and experimental results.

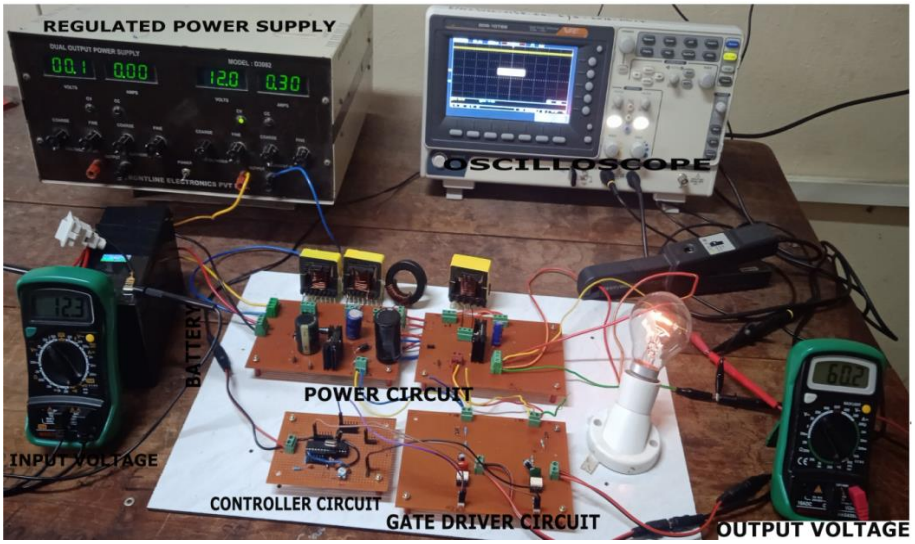


Figure 26. *Hardware implementation of the proposed converter*

Table 4. *Specifications of components and parameters used in hardware setup*

Components	Specifications
Battery	12 V, 7.5 Ah
Regulated Power Supply Unit	(0 – 24) V, 2 A
MOSFET switches S_1 & S_2	2SK2645 N-Channel: 600 V, 9 A (each)
Diodes D_1, D_2, D_3, & D_4	UF5408: 1000 V, 3 A (each)
Controller	dsPIC30F2010
MOSFET Driver	TLP250H
Inductors L_1, L_2, L_3, L_0	1 mH each
Capacitor C_1	100 µF
Capacitors C_2, C_3	10 µF each
Capacitor C_0	1000 µF
Lamp load	60 W
Switching frequency (f_s)	15 kHz
Duty cycle (k) of MOSFET switches S_1 & S_2	0.6 each

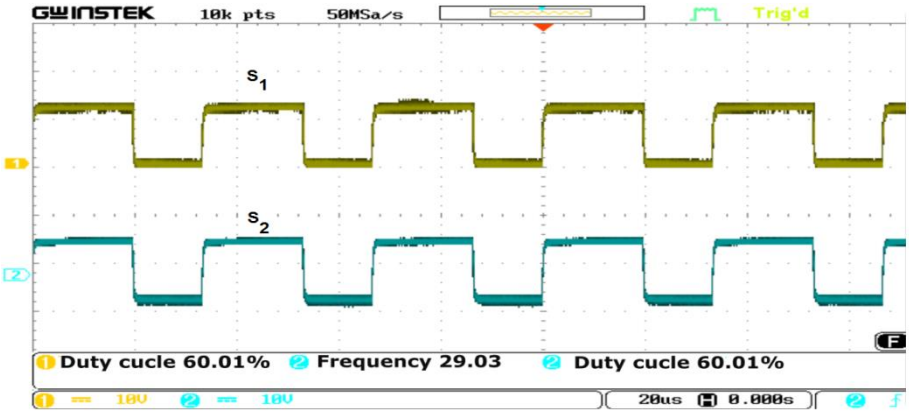


Figure 27. *Gate drive signals for the MOSFET switches S_1 and S_2*

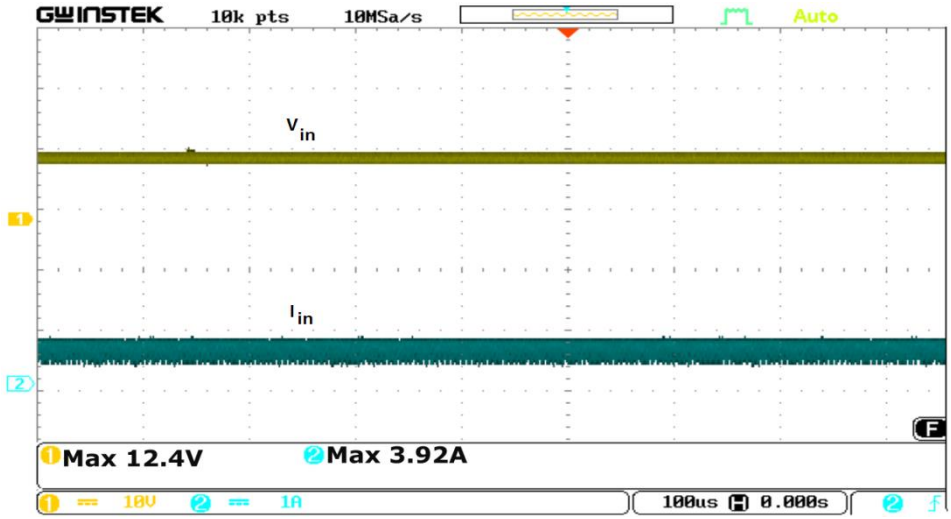


Figure 28. *Voltage (V_{in}) and current (I_{in}) plots on the input side of the modified Cuk structure*

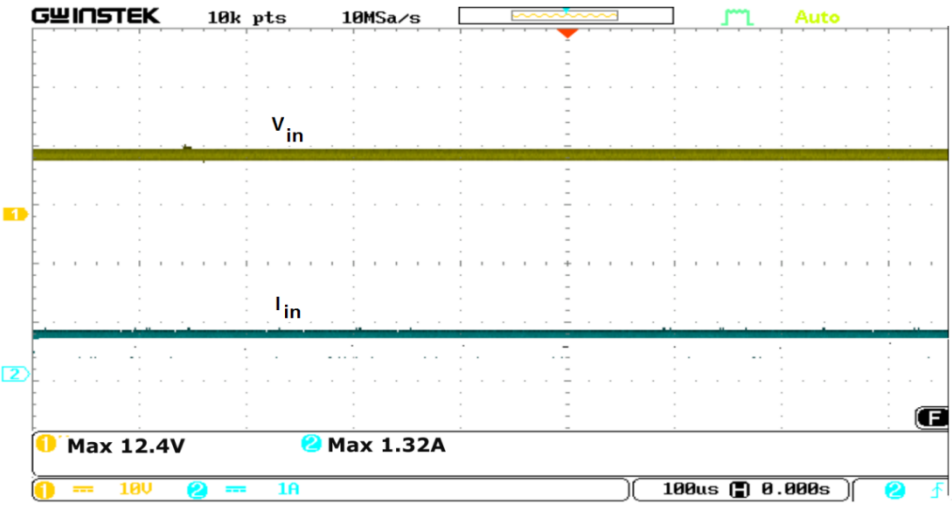


Figure 29. *Voltage (V_{in}) and current (I_{in}) plots on the input side of the SEPIC converter*

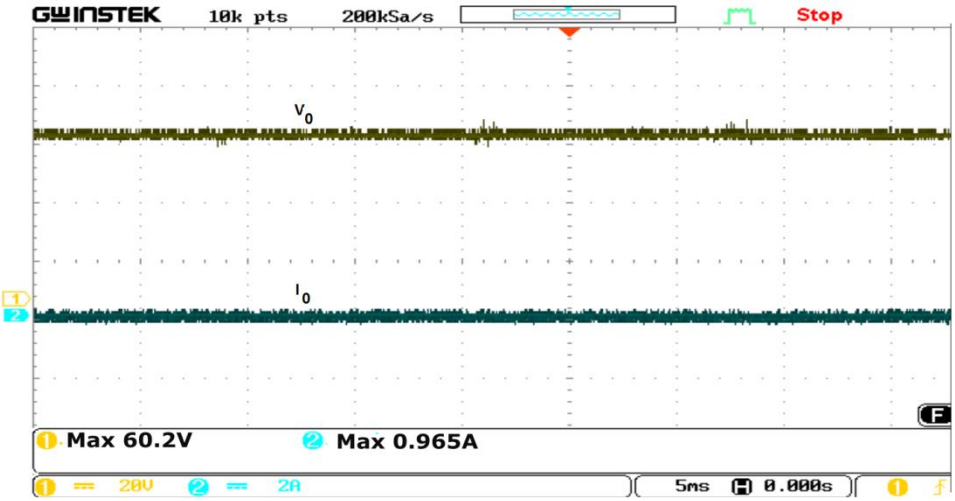


Figure 30. *Load voltage (V_0) and load current (I_0) plots of the proposed hybrid structure*

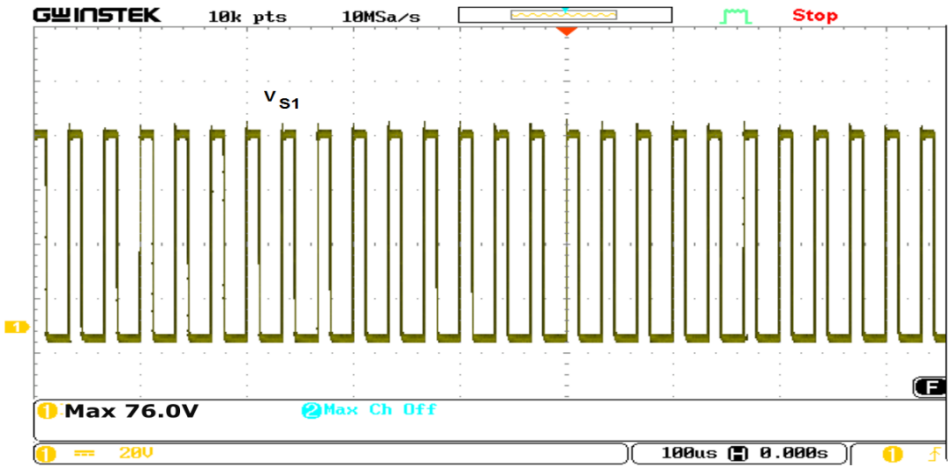


Figure 31. *Measured Voltage stress (V_{S1}) across MOSFET switch S_1*

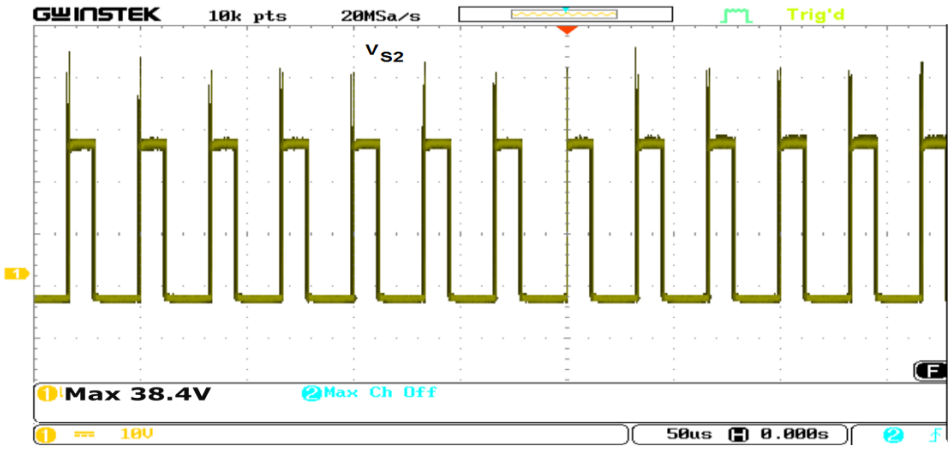


Figure 32. *Measured Voltage stress (V_{S2}) across MOSFET switch S_2*

Table 5*. A comparison between MATLAB simulation and hardware results of the proposed converter*

Parameters	Simulation results	Hardware results
DC input voltage to each converter (V_{in})	12 V	12.4 V
DC output voltage (V_0)	61.6 V	60.2 V
DC output current (I_0)	0.98 A	0.965 A
Duty cycle (k) of the switches S_1 & S_2	0.6 each	0.6 each
Maximum Switch voltage stress (V_{S1} & V_{S2})	76.5 V & 39 V	76 V & 38.4 V

4. CONCLUSION

This research proposal explores the theoretical steady-state behavior, the simulation performance and experimental validation of a transformer-less high step-up gain configured DC-DC power conversion scheme composed of traditional SEPIC and modified Cuk topologies. Two DC sources, each of 12 V, are applied to the proposed integrated structure at a switching frequency 15 kHz and duty cycle ratio of 0.6 for testing its performance using MATLAB / SIMULINK model. The projected converter topology includes certain positive features such as simple control technique, high step-up voltage conversion ratio, continuous inductor current on input side, non-inverting load voltage, and diminished voltage stress across the controlled and uncontrolled power semiconductor based components. Moreover, the enhanced voltage conversion ratio is achievable at low duty cycle ratio itself. A hardware setup of the proposed integrated converter topology is also implemented to validate its performance. The prototype model is also tested with a source voltage of 12 V (DC) at 60% duty factor and 30 kHz switching frequency. The results of simulation and experimental study are compared for the suggested topology. The suggested hybrid topology is found in certain applications that include renewable energy based power generation system and electric vehicles.

CONFLICTS OF INTEREST

No conflict of interest was declared by the author.

REFERENCES

[1] Khan, Y., Liu, F., "Consumption of energy from conventional sources a challenge to the green environment: Evaluating the role of energy imports, and energy intensity in Australia", Environmental Science and Pollution Research, 30: 22712-22727, (2023). DOI: https://doi.org/10.1007/s11356-022-23750-x

[2] Kumar, R., Ojha, K., Ahmadi, M. H., Raj, R., Aliehyaei, M., Ahmadi, A., Nabipour, N., "A review status on alternative arrangements of power generation energy resources and reserve in India", International Journal of Low-Carbon Technologies, 15(2): 224-240, (2020). DOI: https://orcid.org/0000-0002-0097-2534

[3] Erdiwansyah, Mahidin, Husin, H., Nasaruddin, Zaki, M., Muhibbuddin. "A critical review of the integration of renewable energy sources with various technologies", Protection and Control of Modern Power Systems, 6(3): 1-18, (2021). DOI: https://doi.org/10.1186/s41601-021-00181-3

[4] Laveyne, J. I., Bozalakov, D., Eetvelde, G. V., Vandevelde, L., "Impact of solar panel orientation on the integration of solar energy in low-voltage distribution grids", International Journal of Photoenergy, 2020: 1-13, (2020). DOI: https://doi.org/10.1155/2020/2412780

[5] Sutikno, T., Purnama, H. S., Widodo, N. S., Sanjeevikumar, P., Sahid, M. R., "A review on non-isolated low-power DC-DC converter topologies with high output gain for solar photovoltaic system applications", Clean Energy, 6(4): 557-572, (2022). DOI: https://doi.org/ 10.1093/ce/zkac037

[6] Mumtaz, F., Yahaya, N. Z., Meraj, S. T., Singh, B., Ramani Kannan, Ibrahim, O., "Review on non-isolated DC-DC converters and their control techniques for renewable energy applications", Ain Shams Engineering Journal, 12(4): 3747-3763, (2021). DOI: https://doi.org/10.1016/j.asej.2021.03.022

[7] Shin, S. U., "An analysis of non-isolated DC-DC converter topologies with energy transfer media", Energies, 12(8): 1-19, (2019). DOI: https://doi.org/10.3390/en12081468

[8] Abbas, F. A., Abdul-Jabbar, T. A., Obed, A. A., Kersten, A., Kuder, M., Weyh, T., "A comprehensive review and analytical comparison of non-isolated DC-DC converters for fuel cell applications", Energies, 16(8): 1-34, (2023). DOI: https://doi.org/10.3390/en16083493

[9] Sutikno, T., Aprilianto, R. A., Purnama, H. S., "Application of non-isolated bidirectional DC-DC converters for renewable and sustainable energy systems: a review", Clean Energy, 7(2): 293-311, (2023). DOI: https://doi.org/10.1093/ce/zkac070

[10] Supriya, J., Rajashekar, J. S., "A comprehensive review of various isolated DC-DC converter topologies associated with photovoltaic applications", Recent Advances in Electrical & Electronic Engineering, 15(8): 595-606, (2022). DOI: https://doi.org/10.2174/2352096515666220707115544

[11] Meshael, H., Elkhateb, A., Best, R., "Topologies and design characteristics of isolated high step-up DC-DC converters for photovoltaic systems", Electronics, 12(18): 1-42, (2023). DOI: https://doi.org/10.3390/electronics12183913

[12] Murali, D., Shruthi, K., "A non-isolated modified Zeta converter-fed DC motor under load condition", Brazilian Archives of Biology and Technology, 67(1): 1-12, (2024). DOI: https://doi.org/10.1590/1678-4324-2024230420

[13] Gupta, P. P., Kishore, G. I., Tripathi, R. K., "Non-isolated high step-up in voltage DC-DC converter topology for renewable applications", Journal of Circuits, Systems and Computers, 30(6): 1-27, (2021). DOI: https://doi.org/10.1142/S0218126621500936

[14] Niu, J., Tang, Y., "A family of single-switch wide-gain converters with low voltage stress", Energy Reports, 9(10): 1032-1041, (2023). DOI: https://doi.org/10.1016/j.egyr.2023.05.199

[15] Zaid, M., Khan, S., Siddique, M. D., Sarwar, A., Ahmad, J., Sarwer, Z., Iqbal, A., "A transformerless high gain dc–dc boost converter with reduced voltage stress", International Transactions on Electrical Energy Systems, 31(5): 1-17, (2021). DOI: https://doi.org/10.1002/2050-7038.12877

[16] Alhurayyis, I., Elkhateb, A., Morrow, D. J., "Isolated and non-isolated DC-to-DC converters for medium voltage DC networks: A review", IEEE Journal of Emerging and Selected Topics in Power Electronics, 9(6): 7486-7500, (2021). DOI: https://doi.org/10.1109/JESTPE.2020.3028057

[17] Gnanavadivel, J., Jayanthi, K., Nivethini, M., Thejhaswiniy, S. J., Ilakkiya, R., "Implementation of non-isolated high-gain DC-DC converter for electric vehicle application", International Journal of Electronics, 111(11): 1980-2001, (2024). DOI: https://doi.org/10.1080/00207217.2023.2248656

[18] Sugali, H., Sathyan, S., Merlin Mary, N. J., "Design and analysis of quasi-resonant high-gain impedance source DC-DC converter for DC microgrid", International Journal of Electronics, 111(12): 2159-2179, (2024), DOI: https://doi.org/10.1080/00207217.2023.2248667

[19] Saravanan, S., Babu, N. R., "A modified high step-up non-isolated DC-DC converter for PV application", Journal of Applied Research and Technology, 15(3): 242-249, (2017). DOI: https://doi.org/10.1016/j.jart.2016.12.008

[20] Premkumar, M., Subramaniam, U., Alhelou, H. H., Siano, P., "Design and development of non-isolated modified SEPIC DC-DC converter for high-step-up applications: Investigation and hardware implementation", Energies, 13(15): 1-27, (2020). DOI: https://doi.org/10.3390/en13153960

[21] Zhu, B., Liu, J., Liu, Y., Zhi, S., Zhao, Y., "A high-reliability SEPIC converter with reconfigurable voltage conversion gain", Energy Reports, 9(7): 523-531, (2023). DOI: https://doi.org/10.1016/j.egyr.2023.04.160

[22] Gules, R., dos Santos, W. M., dos Reis, F. A., Romaneli, E. F. R., Badin, A. A., "A modified SEPIC converter with high static gain for renewable applications", IEEE Transactions on Power Electronics, 29(11): 5860-5871, (2014). DOI: https://doi.org/10.1109/TPEL.2013.2296053

[23] Jyothi, B., Bhavana, P., Rao, B. T., Pushkarna, M., Kitmo Djidimbele, R., "Implementation of modified SEPIC converter for renewable energy built DC microgrids", International Journal of Photoenergy, 2023: 1-13, (2023). DOI: https://doi.org/10.1155/2023/2620367

[24] Gao, S., Wang, Y., Guan, Y., Xu, D., "A high-frequency high voltage gain modified SEPIC with integrated inductors", IEEE Transactions on Industry Applications, 55(6): 7481-7490, (2019). DOI: https://doi.org/10.1109/TIA.2019.2909498

[25] Haider, Z., Ulasyar, A., Khattak, A., Zad, H. S., Mohammad, A., Alahmadi, A. A., Ullah, N., "Development and analysis of a novel high-gain CUK converter using voltage-multiplier units", Electronics, 11(17): 1-16, (2022). DOI: https://doi.org/10.3390/electronics11172766

[26] Joseph, K. D., Daniel, A. E., Unnikrishnan, A., "Modified interleaved Cuk converter with improved voltage gain and reduced THD", Arabian Journal for Science and Engineering, 48(5): 6137-6147, (2023). DOI: https://doi.org/10.1007/s13369-022-07251-0

[27] Shayeghi, H., Mohajery, R., Hosseinpour, M., Sedaghati, F., Bizon, N., "A transformer-less high voltage gain DC-DC converter based on Cuk converter and voltage-lift technique", Journal of Energy Management and Technology, 8(1): 23-34, (2024). DOI: https://doi.org/10.22109/jemt.2023.416222.1470

[28] Chen, H., Lin, W. M., Liu, W. R., He, W., "Tapped-inductor bi-directional Cuk converter with high step-up/down conversion ratio and its optimum design", Scientific Reports, 12: 1-16, (2022). DOI: https://doi.org/10.1038/s41598-022-17801-z

[29] Mahafzah, K. A., Al-Shetwi, A. Q., Hannan, M. A., Babu, T. S., Nwulu, N., "A new Cuk-based DC-DC converter with improved efficiency and lower rated voltage of coupling capacitor", Sustainability, 15(11): 1-17, (2023). DOI: https://doi.org/10.3390/su15118515

[30] Murali, D., "A transformerless boost-modified Cuk combined single-switch DC-DC converter topology with enhanced voltage gain", Brazilian Archives of Biology and Technology, 66(3/4): 1-20, (2023). DOI: https://doi.org/10.1590/1678-4324-2023220101

[31] Mahafzah, K. A., Obeidat, M. A., Mansour, A., Sanseverino, E. R., Zizzo, G., "A new smart grid hybrid DC-DC converter with improved voltage gain and synchronized multiple outputs", Applied Sciences, 14(6): 1-18, (2024). DOI: https://doi.org/10.3390/app14062274

[32] Ranganathan, S., Mohan, A. N. D., "Formulation and analysis of single switch high gain hybrid DC to DC converter for high power applications", Electronics, 10(19): 1-14, (2021). DOI: https://doi.org/10.3390/electronics10192445

[33] Karthikeyan, M., Elavarasu, R., Ramesh, P., Bharatiraja, C., Sanjeevikumar, P., Mihet-Popa, L., Mitolo, M., "A hybridization of Cuk and Boost converter using single switch with higher voltage gain capability", Energies, 13(9): 1-24, (2020). DOI: https://doi.org/10.3390/en13092312

[34] Li, H., Cheng, L., Sun, X., Li, C., "High step-up combined boost-Cuk converter with switched-inductor", IET Power Electronics, 15(15): 1664-1674, (2022). DOI: https://doi.org/10.1049/pel2.12335

[35] Priyadarshi, N., Bhaskar, M. S., Padmanaban, S., Blaabjerg, F., Azam, F., "New CUK-SEPIC converter based photovoltaic power system with hybrid GSA-PSO algorithm employing MPPT for water pumping applications", IET Power Electronics, 13(13): 2824-2830, (2020). DOI: https://doi.org/10.1049/iet-pel.2019.1154

[36] Murali, D., "Closed-loop implementation of a non-isolated high step-up integrated SEPIC-CUK DC-DC converter structure with single switch", Brazilian Archives of Biology and Technology, 67(2): 1-15, (2024). DOI: https://doi.org/10.1590/1678-4324-2024230787