# Circuit Implementation and PRNG Applications of Time Delayed Lorenz System

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**ABSTRACT** In this study, time delayed form of Lorenz system is introduced, and exemplary applications of the time delayed Lorenz system are performed. Firstly, the time delayed Lorenz system is numerically solved by considering the Lorenz system as a system of time delayed differential equations. Then, time series and phase portraits of the state variables of the time delayed system are obtained. After then, circuit implementation of the time delayed system is carried out with discrete analog components. Finally, a random number generator application is carried out by selecting different number of bits obtained from the state variables of the time delayed system. The results of all the applications are sufficiently good that the time delayed system can be used in engineering applications.

## INTRODUCTION

There are many new chaotic systems proposed in the literature after chaos phenomenon and chaotic systems are emerged as a field of study. However, the Lorenz system, one of the most popular chaotic system, has been still studied (Lorenz 1963). Although the Lorenz system retains its popularity, the use of the Lorenz chaotic system in engineering applications like circuit implementation is not very easy. Moreover, the introduction of different time delay for each state variable will make harder to solve the system numerically and to implement as a circuit. In this study, different amount of time delays for each state variable is considered.

Time delayed differential equations are very important for chaotic systems and their engineering applications (Hale and Lunel 2013). Hence, there are many different studies of time delayed chaotic systems in the literature. For example, stability analyses of time delayed differential equations were discussed (Deng *et al.* 2006). There are also studies of synchronization of such time delayed systems (Cheng *et al.* 2008). In another study, a time delayed chaotic system was obtained from Logistic-map system (Acho 2017). In (Qin-Qin 2015), a parameter defining problem was considered for a general time delayed chaotic system and its analyses were performed. In (Pham *et al.* 2016), a novel time delayed chaotic

system with hidden attractors was proposed. A parameter defining problem was investigated in (Tang *et al.* 2009) to determine unknown parameters of a time delayed chaotic system. There are also studies in which applications of time delayed systems were realized for sliding-mod (Liu and Yang 2015) and active control (Tang 2014).

If the realized engineering applications of the chaotic systems are investigated, the most of these applications are focused on circuit implementation (Pehlivan *et al.* 2019; Adiyaman *et al.* 2020; Kacar *et al.* 2018; Jahanshahi *et al.* 2018; Liu *et al.* 2020) and random number generator (RNG) (Akgul *et al.* 2019; Moysis *et al.* 2020; Alcin *et al.* 2021; Agarwal 2021; Kaçar 2016; Vaidyanathan *et al.* 2018). Accordingly, it will be sufficient to realize these two applications of a proposed chaotic system to show the usability of the chaotic system in engineering applications. Hence, a circuit implementation and RNG applications of the proposed Time Delayed Lorenz System (TDLS) are realized in this study. The contribution of this study to the literature can be explained as follows. In this study, the different time delays are used for each state variable simultaneously and chaotic behaviour is observed after solving the time delayed differential equations numerically. Then, to the best of the authors' knowledge, a time delayed chaotic system is modelled using discrete circuit components for the first time in the literature. Finally, four different pseudo random number generator (PRNG) applications are realized by selecting different bits of the state variables.

The organization of the article is as follows. In the second section, the proposed TDLS is introduced. In the third section, circuit implementation of the TDLS is given. In the fourth section, the PRNG applications of the TDLS are presented. Finally, conclusion is given in the fifth section.

## TIME DELAYED LORENZ SYSTEM

In this section, the time delayed form of Lorenz chaotic system is presented. The time delayed Lorenz system (TDLS) is given in Equation 1. The most important aspect of the proposed system is that each state variable has a different amount of time delay.

$$\dot{x} = a(y(t - \tau_y) - x(t - \tau_x))$$
$$\dot{y} = x(t - \tau_x)(b - z(t - \tau_z)) - y(t - \tau_y) \quad (1)$$
$$\dot{z} = x(t - \tau_x)y(t - \tau_y) - cz(t - \tau_z)$$

Equation 1, the system parameters are $a = 10$, $b = 28$, and $c = 8/3$, the initial conditions are $x(0) = 10$, $y(0) = -10$, and $y(0) = 15$, the time delays are $\tau_x = 0.0014$, $\tau_y = 0.01$, and $\tau_z = 0.05$. The obtained time series and phase of the TDLS when numerically solved for these given values are given in Figure 1 and 2, respectively. The used algorithm for numerical solution of Equation 1 tracks discontinuities and integrates with the explicit Runge-Kutta (2,3) pair and interpolant (Shampine and Thompson 2001; Jacek Kierzenka and Thompson 2021). Also, in the used numerical solution, the step intervals are selected longer than the (Shampine and Thompson 2001; Jacek Kierzenka and Thompson 2021).

When Figure 1 is examined, it can be said that the obtained time series of the TDLS are varied randomly and nonperiodically. When Figure 2 is examined, it can be said that the orbits of the phase portraits in accordance with chaotic behaviour and the phase portraits of TDLS are very different from the original Lorenz system. Accordingly, the system exhibits chaotic behaviour for the given parameters, initial conditions, and time delay values and it is understood that the time delays introduce differences in the dynamical behaviour of the system.
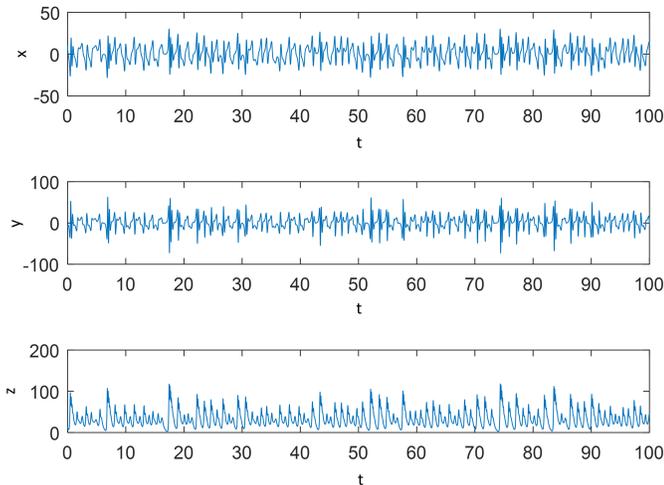


**Figure 1** Time series of the state variables
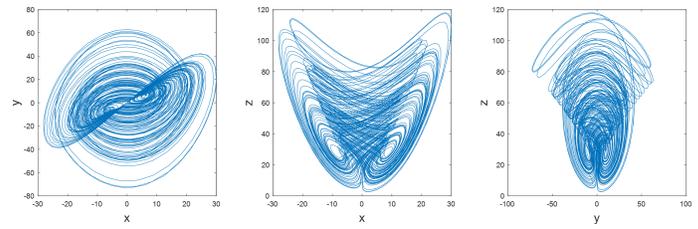


**Figure 2** Phase portraits of the state variables

## CIRCUIT IMPLEMENTATION

In this section, circuit implementation of the TDLS is given. In the literature, there are many studies in which the chaotic systems were realized with electronic circuits (Pehlivan *et al.* 2019; Adiyaman *et al.* 2020; Kacar *et al.* 2018; Jahanshahi *et al.* 2018; Liu *et al.* 2020). However, to the best of the authors' knowledge, there are no circuit implementation of time delayed chaotic systems in the literature. In this paper, electronic circuit implementation of the time delayed circuit is achieved.

The circuit for the time delay is given in Figure 3. Time delay is realized with a source follower and an LC circuit as shown in Figure 3. In the figure $x(t)$ is the state variable and $x(t - d)$ is the time delayed form of $x(t)$ by $d$ seconds.
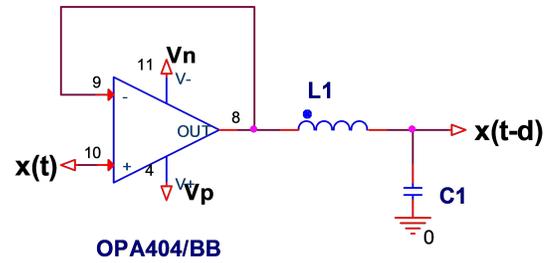


**Figure 3** Time delay circuit

In the circuit, the time delay in seconds is

$$d = \sqrt{L_1 C_1} \quad (2)$$

and the time delay must be lesser than or equal to one over the bandwidth of the signal $x(t)$ since the LC circuit will suppress higher frequency terms greater than $\frac{1}{\sqrt{L_1 C_1}}$.

$$d \leq 1/B_{x(t)} \quad (3)$$

Here $B_{x(t)}$ is bandwidth of the signal in $rad/s$.

Before the circuit implementation of the TDLS, the state variables of the TDLS must be scaled as it is seen in Figure 1 that the amplitude of the state variables are quite high. The state variable $x, y$, and $z$ are scaled down by the factor of 5,10, and 20, respectively. Since the state variables are scaled down, the initial values are also scaled down by the same factors. Hence, the initial conditions are $x(0) = 2$, $y(0) = -1$, and $y(0) = 0.75$ for the circuit implementation.

For the scaling process of the state variables, let $X = x/5$, $Y = y/10$, and $Z = z/20$. Then, the time derivatives are $\dot{X} = \dot{x}/5$, $\dot{Y} = \dot{y}/10$, and $\dot{Z} = \dot{z}/20$. By inserting these new state variables into Equation 1, the system becomes

$$5\dot{X} = a(10Y(t - \tau_y) - 5X(t - \tau_x))$$
$$10\dot{Y} = 5X(t - \tau_x)(b - 20Z(t - \tau_z)) - 10Y(t - \tau_y) \quad (4)$$
$$20\dot{Z} = 5X(t - \tau_x)10Y(t - \tau_y) - c20Z(t - \tau_z)$$

By rearranging Equation 4, the scaled TDLS becomes

$$\dot{X} = a(2Y(t - \tau_y) - X(t - \tau_x))$$
$$\dot{Y} = 0.5X(t - \tau_x)(b - 2Z(t - \tau_z)) - Y(t - \tau_y) \quad (5)$$
$$\dot{Z} = 0.125X(t - \tau_x)Y(t - \tau_y) - cZ(t - \tau_z)$$

After scaling process of the state variables, the system is scaled up in the frequency domain by the factor of 2500 to increase bandwidth of the state variables and to decrease the run time of the circuit. Since the frequency spectrum of the state variables are scaled up by the factor of 2500, the time delays are scaled down by the same factor. The circuit realization of system in Equation 5 is realized for the system parameters values $a = 10$, $b = 28$, and $c = 8/3$, the initial conditions are $x(0) = 2$, $y(0) = -1$, and $y(0) = 0.75$, the time delays are $\tau_x = 0.4\mu s$, $\tau_y = 4\mu s$, and $\tau_z = 20\mu s$. The complete circuit realization of the system is given in Figure 4.
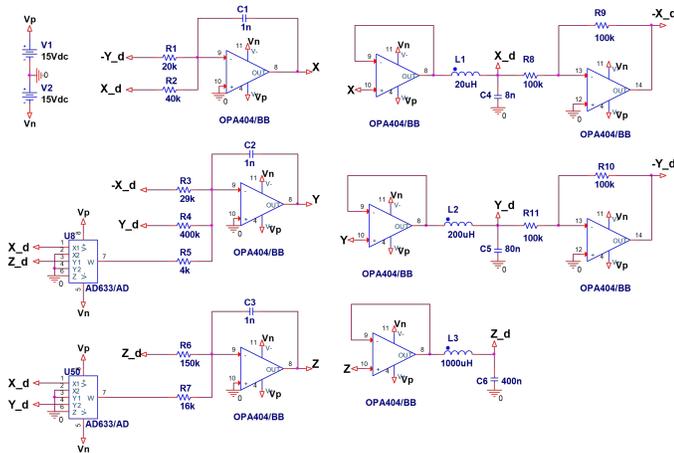


**Figure 4** Circuit implementation of the time delayed Lorenz system for the system parameters values $a = 10$, $b = 28$, and $c = 8/3$, the initial conditions are $x(0) = 2$, $y(0) = -1$, and $y(0) = 0.75$, the time delays are $\tau_x = 0.4\mu s$, $\tau_y = 4\mu s$, and $\tau_z = 20\mu s$s

In the circuit, $R_1 = 20k\Omega$, $R_2 = 40k\Omega$, $R_3 = 29k\Omega$, $R_4 = 400k\Omega$, $R_5 = 4k\Omega$, $R_6 = 150k\Omega$, $R_7 = 16k\Omega$, $R_8 = R_9 = R_10 = R_11 = 100k\Omega$, $L_1 = 20\mu H$, $L_2 = 200\mu H$, $L_3 = 1000\mu H$, $C_1 = C_2 = C_3 = 1nF$, $C_4 = 8nF$, $C_5 = 80nF$, $C_6 = 400nF$.

The time series and phase portraits obtained from the simulation of the circuit in Figure 4 are given in Figure 5 and 6, respectively. The simulation is performed on ORCAD-PSpice platform.
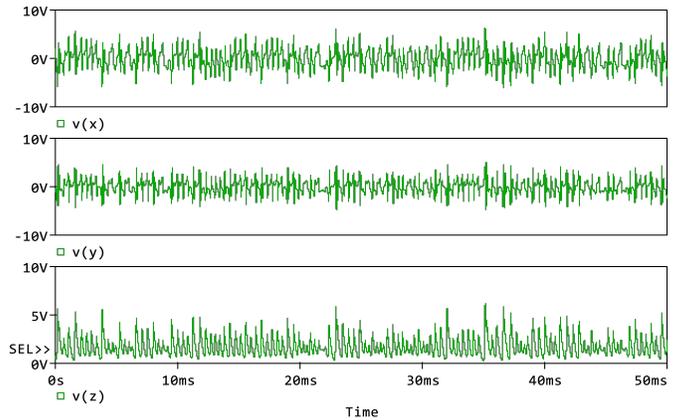


**Figure 5** The time series of the delayed Lorenz system for the system parameters values $a = 10$, $b = 28$, and $c = 8/3$, the initial conditions are $x(0) = 2$, $y(0) = -1$, and $y(0) = 0.75$, the time delays are $\tau_x = 0.4\mu s$, $\tau_y = 4\mu s$, and $\tau_z = 20\mu s$s
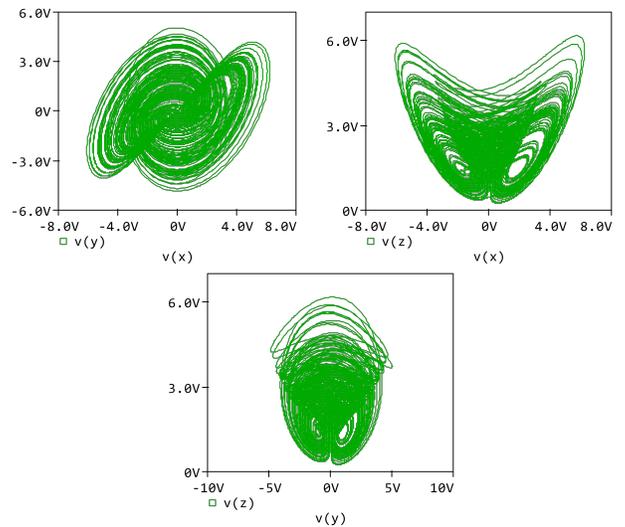


**Figure 6** The phase portraits of the delayed Lorenz system for the system parameters values $a = 10$, $b = 28$, and $c = 8/3$, the initial conditions are $x(0) = 2$, $y(0) = -1$, and $y(0) = 0.75$, the time delays are $\tau_x = 0.4\mu s$, $\tau_y = 4\mu s$, and $\tau_z = 20\mu s$s

If the time series and phase portraits obtained from the spice simulation are compared with the time series and the phase portraits obtained from solving the TDLS numerically, it can be said that the circuit implementation of the TDLS is realized accurately.

## PRNG APPLICATIONS

In this section, the realization of four different PRNG designs are given. The PRNGs are obtained by solving the TDLS given in Equation 1 numerically. In each designed PRNG, different bit series obtained from the state variables of the TDLS are used. The flowchart of the PRNG designs is given in Figure 7. As it is seen in Figure 7, the state variables are obtained by solving the system numerically, after setting the system parameters, initial conditions, and time delays values. The state variables obtained by numerical calculations are in floating point format are converted into 32 bits binary format. Then, the random number bit series are obtained by selecting certain appropriate number of least significant bits (LSBs). Here, each PRNG is designed from different state variables and with selecting different number of LSBs. In this study, four different PRNGs are designed with this approach. For the design of PRNG-1, a random bit series is generated by selecting the first LSB from each state variable ($x,y,z$). For the design of PRNG-2, PRNG-3, and PRNG-4, a random bit series is generated by selecting the first four LSBs from each state variables $x,y$, and $z$, respectively. For every PRNG, NIST-800-22 statistical tests (Bassham *et al.* 2010) are performed when the size of the generated bit series are reached 1000000 bits which is required by the NIST tests.

The NIST test results for all the generated PRNGs are given in Table 1. For a bit series to pass successfully from each NIST test, the *P*-value obtained in each test must be between 0.001 and 1 ($1 > P\text{-value} > 0.001$). Here *P*-value is the probability that a perfect RNG would have generated a sequence less random than the sequence that was tested. The *P*-value equals to 1 indicates that the sequence has perfect randomness, whereas *P*-value equals to 0 indicates that the sequence is completely non-random. Furthermore, when the *P*-value $\geq 0.001$, the sequence is considered as random with a confidence of 99.9%(Bassham *et al.* 2010). All the NIST tests are performed on MATLAB environment.

If the results given in Table 1. are examined, it can be said that all the designed PRNGs pass all the NIST tests successfully. Accordingly, the proposed TDLS in Equation 1. has sufficient randomness that it can be used in data security applications.
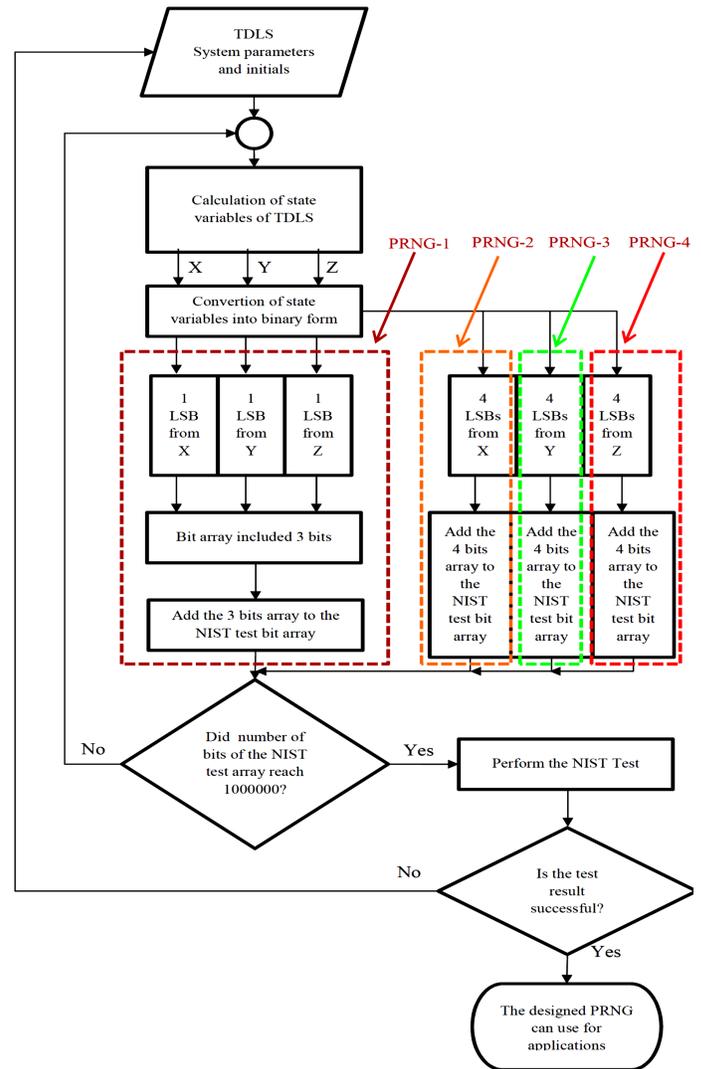


**Figure 7** Flow diagram of the designed PRNGs

**Table 1 NIST-800-22 test results of TDLS based PRNGs**

| Statistical Tests | PRNG -1 | PRNG -2 | PRNG -3 | PRNG -4 | Results |
|---|---|---|---|---|---|
| Frequency (Monobit) Test | 0.227047262346928 | 0.939419098199487 | 0.452051058788007 | 0.74896833055336 | Successful |
| Block-Frequency Test | 0.420199408706029 | 0.12683780891 | 0.25828539912 | 0.18496247976 | Successful |
| Cumulative-Sums Test | 0.40154501916006 | 0.954262689644538 | 0.657794646611129 | 0.580632315828042 | Successful |
| Runs Test | 0.809910815227043 | 0.78561757692 | 0.45239095310 | 0.20333669229 | Successful |
| Longest-Run Test | 0.699072314072508 | 0.0593326790453765 | 0.071698278949431 | 0.581605726274521 | Successful |
| Binary Matrix Rank Test | 0.567418552088598 | 0.29417664507 | 0.36806531540 | 0.49848122628 | Successful |
| Discrete Fourier Transform Test | 0.0183542134338342 | 0.186356486587195 | 0.0310440276996156 | 0.659590791427404 | Successful |
| Non-Overlapping Templates Test | 0.0910820098687739 | 0.04581818944 | 0.00265744608 | 0.03188609869 | Successful |
| Overlapping Templates Test | 0.554865280067303 | 0.669055771344141 | 0.532900762615005 | 0.247345441097719 | Successful |
| Maurer's Universal Statistical Test | 0.679570957855461 | 0.80734843081 | 0.08350574528 | 0.92319905938 | Successful |
| Approximate Entropy Test | 0.639684970544748 | 0.106378560917655 | 0.650943909676795 | 0.117260917143001 | Successful |
| Random-Excursions Test (x = -4) | 0.703450581514076 | 0.37281099664 | 0.16507680806 | 0.28180552081 | Successful |
| Random-Excursions Variant Test (x = -9) | 0.900334238396749 | 0.301103909474349 | 0.274949621155743 | 0.26897769139 | Successful |
| Serial Test-1 | 0.498246191923405 | 0.13739086594 | 0.24094191226 | 0.51233919246 | Successful |
| Serial Test-2 | 0.703867335568016 | 0.172244663440799 | 0.324188206506017 | 0.539500232899045 | Successful |
| Linear-Complexity Test | 0.1748830988160720 | 0.98952603429 | 0.91278048851 | 0.46910323363 | Successful |

## CONCLUSIONS

In this study, the time delay form of Lorenz system which is one of the most known and popular chaotic system is presented. The most important aspect of the proposed time delayed system in here is that the system still exhibits chaotic behaviour with different dynamical properties after introducing different time delay to each state variable. The first important result of this study is that observing chaotic behaviour of the time delayed system by solving numerically.

The most important contribution of this study to the literature is successful analog circuit realization of time delayed system with three different time delays. As it can be seen from the obtained time series and phase portraits in MATLAB and PSpice environments, the circuit realization of the time delayed chaotic system is successful. Another important application realized in this study is designing four different PRNGs by selecting different number of LSBs of the state variables. Moreover, all the designed PRNGs pass the NIST tests successfully. According to the NIST tests results all the generated bit series have considered to be random with a confidence of 99.9%. This shows that, the designed RNGs are suitable for multimedia security applications. As a result, the exhibition of the chaotic behaviour of the proposed system is proved with all the successfully realized applications and this shows that the proposed system can be used in engineering applications.

### Conflicts of interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

### Availability of data and material

Not applicable.

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