MOS Transistor Based Low Power and High Speed Fundamental Logic Gates

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Abstract: In this paper, low voltage, low power, high speed and full swing, 1V MOS transistor based fundamental logic gates at 1GHz operation frequency are examined. The main purpose of this work is to comprehend basic ideas related to logic gate and circuit design research field and lay the foundation for novel design methods. The other purpose is to show that these full swing logic gates can be performed under low voltage and high speed conditions. Furthermore, MOS transistor based non-full swing logic gates and how to do them full swing are also examined. Waveforms and numerical results of examined structure's simulations show that MOS transistor based fundamental logic gates can be acquired at 1V supply voltage and 1GHz operation frequency levels. Theoretical results have been confirmed by HSPICE using 65nm CMOS process technology.

Düşük Güçlü ve Yüksek Hızlı MOS Transistörlü Temel Lojik Kapılar

Anahtar Kelimeler
Düşük gerilim,
Düşük güç,
Yüksek hız,
Lojik kapı,
MOS

Öz: Bu çalışmada, düşük gerilimli, düşük güçlü, yüksek hızlı ve tam salınımlı, 1GHz çalışma frekansında 1V MOS transistörlü temel lojik kapılar incelenmiştir. Bu çalışmanın temel amacı lojik kapı ve devre tasarımları araştırma alanı ile ilgili temel fikirleri edinmek ve yeni tasarım metotları için temel oluşturmaktır. Diğer bir amaç ise bu tam salınımlı lojik kapıların düşük gerilim ve yüksek hız şartlarında gerçekleştirilebildiğini göstermektir. Ek olarak, MOS transistörlü tam salınımlı olmayan lojik kapılar ve bunların nasıl tam salınımlı yapılabildiği incelenmiştir. İncelenen yapıların benzetim dalga şekilleri ve nümerik sonuçları, MOS transistörlü temel lojik kapıların 1V besleme gerilimi ve 1GHz çalışma frekansı seviyelerinde elde edilebildiğini göstermektedir. Teorik sonuçlar 65nm CMOS üretim teknolojisini kullanan HSPICE programında doğrulanmıştır.

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1. Introduction

In recent years, in view of big growth in portable electronic devices such as calculators, smart phones, tablets, laptops, the demand for using low voltage and low power, energy efficient and high speed circuits have largely been investigated in very-large-scale-integration (VLSI) systems. Arithmetic units are very important for most of digital designs and logic gates are fundamental building blocks of these kind of units. Accordingly, the fact that performance parameters of logic gates are improved provide more productive entire system working [1,2].

Designs with MOS transistors have significantly replaced designs with BJT transistors. Many papers have been published related to logic gates in the literature using MOS transistors [2-6] or advanced design methods. Some of them are DTMOS (Dynamic Threshold-voltage MOS) [7,8], FGMOS (Floating Gate MOS) [9,10] and CNTFET (Carbon Nano Tube FET) based digital design methods [11,12]. So, the fact that MOS transistor based fundamental logic gates are performed provide better understanding for novel and advanced designs.

The logic gates perform same functions regardless of design methods but their main performance parameters which are power dissipation, propagation delay and PDP (power-delay product) are different due to design methods. The most common approach for reducing power dissipation is power supply voltage scaling. However, there are two main parameters to consider important when reducing supply voltage. First, minimum values of transistor canal region parameters (W, width and L, lenght) values are should also be reduced [1]. Second, reduced supply voltage should be more than threshold voltage of transistor two or three times at least [13,14].

In this work, MOS transistor based fundamental logic gates are examined. Firstly, they are seperated into two groups as full swing or non-full swing. While full swing ones generates strong (logic 0 or logic 1) values at the output, the other generates weak (logic near intermediate values). Some properties of these fundamental logic gates, which are transistor count, input-output relation and output defines, are examined. Secondly, full swing MOS transistor based fundamental logic gates are graphically and numerically simulated. Simulation results showed that these gates can be performed at low voltage and high speed operation frequency levels. The common approachs are utilized related to logic gate and circuit design research field and the foundation is laid for novel design methods. Consequently, this work introduces important and common fundamentals and provides a better and faster introduction to the field of digital design methods research.

2. Material and Method

2.1. MOS transistor based fundamental logic gates

Symbols of the eight fundamental logic gates are shown in Figure 1. These eight gates can be designed by using MOS transistors. These MOS transistor based logic gates can be separated into two groups considering that they are full swing or non-full swing. Firstly, NOT-NOR-NAND-XOR-XNOR are known as fundamental logic gates in the literature and provide full swing logic values at the output. At second, BUF-OR-AND are also fundamental but they are non-full swing. Circuit designs of these gates are displayed in Figure 2, Figure 3 and Figure 4, respectively.

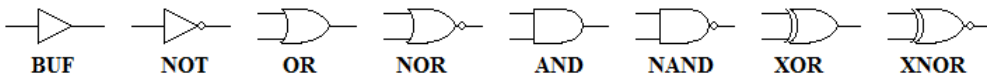

Figure 1. Symbols of the eight fundamental logic gates

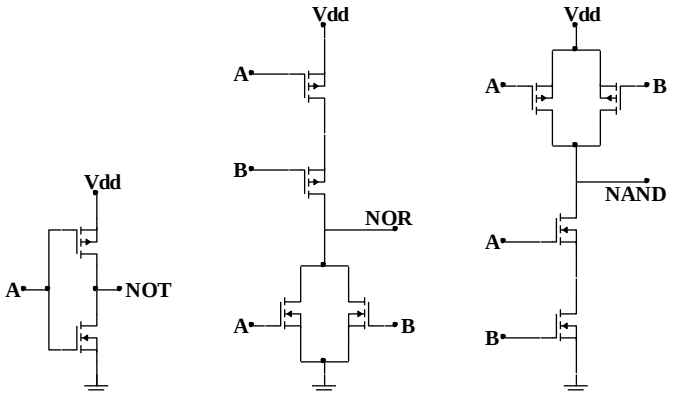

Figure 2. MOS transistor based full swing fundamental logic gates - NOT, NOR, NAND

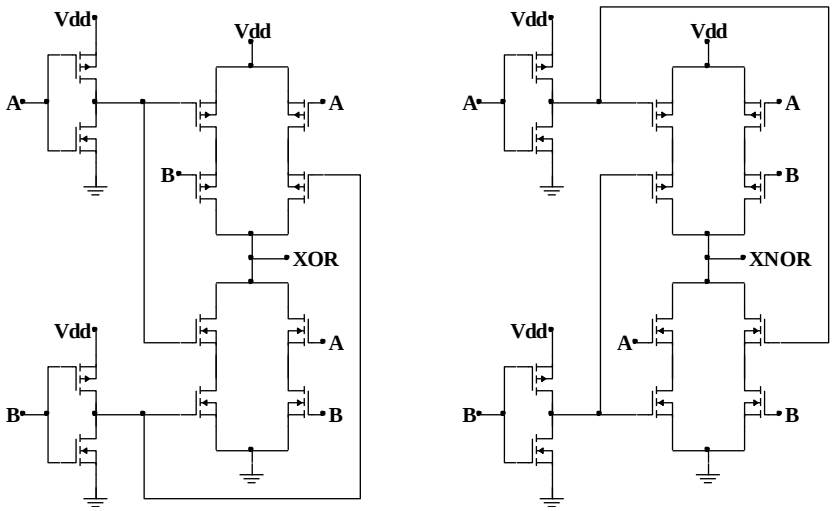

Figure 3. MOS transistor based full swing fundamental logic gates - XOR, XNOR

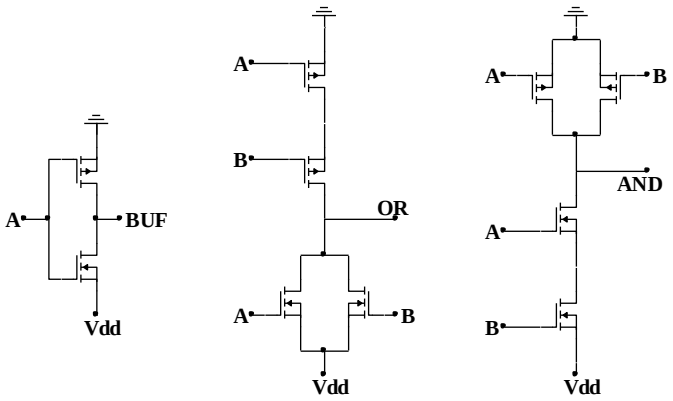

Figure 4. MOS transistor based non-full swing fundamental logic gates - BUF, OR, AND

Some properties of these MOS transistor based fundamental logic gates, which are transistor count, logic states and strong or weak logic values at the output, defines are given in Table 1 and Table 2. While full swing logic gates generates strong logic values at the output, non-full swing ones generates weak. V_{tp} and V_{tn} are the threshold voltages of p-MOS and n-MOS transistors, respectively.

Table 1. Some properties of MOS transistor based full swing fundamental logic gates

Gate	Transistor count	Inputs		Outputs	
		A	B	Result	Define
NOT	2	0/1	-	1/0	strong
NOR	4	0/0/1/1	0/1/0/1	1/0/0/0	strong
NAND	4			1/1/1/0	strong
XOR	12			0/1/1/0	strong
XNOR	12			1/0/0/1	strong

Table 2. Some properties of MOS transistor based non-full swing fundamental logic gates

Gate	Transistor count	Inputs		Outputs		
		A	B	Desired	Result	Define
BUF	2	0/1	-	0/1	$\|V_{tp}\|/(V_{dd}-V_{tn})$	weak
OR	4	0/0/1/1	0/1/0/1	0/1/1/1	$\|2\times V_{tp}\|/(V_{dd}-V_{tn})/(V_{dd}-V_{tn}/2)$	weak
AND	4			0/0/0/1	$\|V_{tp}/2\|/\|V_{tp}\|/\|V_{tp}\|/(V_{dd}-2\times V_{tn})$	weak

BUF-OR-AND logic gates can also be acquired as full swing through a NOT logic gate addition to the output of NOT-NOR-NAND. However, this idea causes to use two more MOS transistors.

3. Results

3.1. Simulation setups

Simulation setups are summarized in Table 3. V_{dd} = positive input voltage is 1V and V_{gnd} = negative input voltage is 0V. Operation frequency is 1GHz. 1V supply voltage is appropriated for 65nm CMOS process technology [1]. According to 65nm, $L_p = L_n$ value is 65nm. p-ratio (W_p/L_p) and n-ratio (W_n/L_n) values of p-MOS and n-MOS transistors are determined as 2 and 1, respectively. The reason of p-ratio > n-ratio is that the transconductance of p-MOS transistor is lower than that of n-MOS transistor.

Table 3. Simulation setups

Parameter	Unit	Value
Vdd = Vi^+	V	1
Vgnd = Vi^-	V	0
Input waveform	-	Square
Input frequency	GHz	1
R (load)	MΩ	1000
Wp / Wn	nm	130 / 65
Lp = Ln	nm	65
p / n	-	2 / 1

3.2. Simulation results

Input-output signals of NOT and NOR-NAND-XOR-XNOR logic gates are indicated in Figure 5 and Figure 6, respectively. As shown in figures, these full swing logic gates generates strong logic values at the output voltage levels. Moreover, power dissipation, propagation delay and PDP values are summarized in Table 4. The graphical and numerical simulations are obtained by using HSPICE.

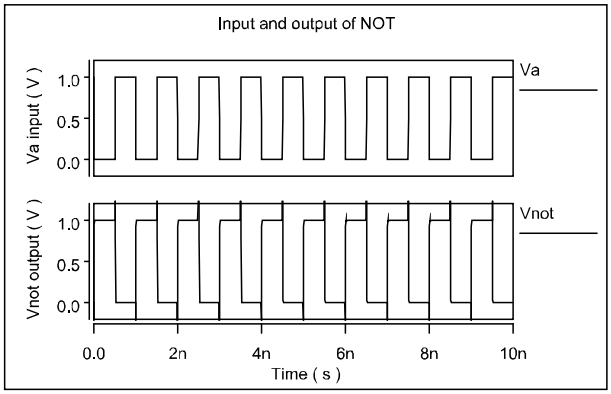

Figure 5. Input-output signals of NOT logic gate

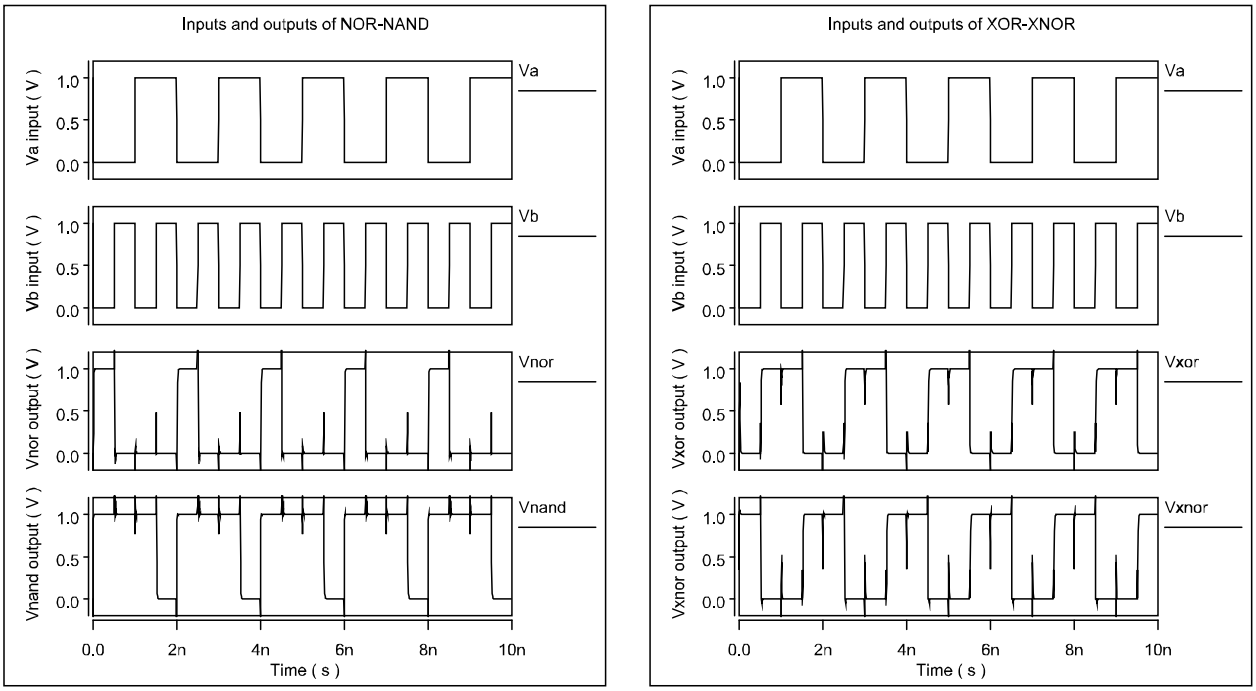

Figure 6. Input-output signals of NOR-NAND-XOR-XNOR logic gates

Table 4. Simulation results

Gate	Power (nW)	Delay (ps)	PDP (10^{-21} J)
NOT	0.859	6.840	5.876
NOR	0.367	11.352	4.166
NAND	1.719	9.524	16.372
XOR	3.435	15.582	53.524
XNOR	3.849	15.982	61.515

4. Discussion and Conclusion

The basic aspect of MOS transistor based fundamental logic gates are examined in this work to achieve better understanding of fundamentals for logic gate and circuit design research field and lay the foundation for novel design methods. Firtsly, they are separated into two groups by evaluating whether full swing or not and the basic properties are introduced. And then, simulations are performed for full swing ones as graphically and numerically. Some of important simulation parameters are 1V supply voltage and 1GHz operation frequency levels. At these levels, it is shown that MOS transistor based fundamental logic gates can be achieved.

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