

Signal Flow Graph – The Right Presentation of an Electrical Circuit[#]

Feim Ridvan RASIM*, Sebastian M. SATTLER

Chair of Reliable Circuits and Systems, LZS, Friedrich-Alexander-University Erlangen-Nuremberg, Paul-Gordan-Str. 5, 91052 Erlangen, Germany, Email: <u>feim.rasim@fau.de,sebastian.sattler@fau.de</u>

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Abstract

In this paper a method called "signal flow graph (SFG)" is presented, which represents a system by its signal flows, in abstract term it is a directed and weighted graph with signals in nodes and functions on edge. The edges of this graph are small processing units which process the incoming signals in specific form and send the result to all outgoing nodes. The SFG allows a good visual inspection into complex feedback problems. Furthermore such a presentation allows for a clear and unambiguous description of a generating system, for example, a netview. A Signal Flow Graph (SFG) allows a fast and practical network analysis based on a clear data presentation in graphic format of the mathematical linear equations of the circuit. During creation of SFGs the Direct Current-Case (DC-Case) was observed since the correct current and voltage directions was drawn from zero frequency. In addition, the mathematical axioms, which are based on field algebra, are declared.

Keywords: Analog Circuit, Transfer Function, Symbolic Analysis, Signal Flow Graph, Network Theory.

1. Introduction

There are diverse methods to calculate transfer functions of electrical circuits such as two-port network theory, nodal analysis method (Schmidt et al. 2006) and time constant method (Gaetano et al. 2003). These methods are generally timeconsuming and computationally intensive. Furthermore, it is always useful to develop a common graphical model, with using this model to make a connection between the state variables (parameters) and the transfer function as well as to obtain a better understanding of the complex functionality of a network. Using mesh rules, node rules and Ohm's equations can a signal flow graph set up. Targeted minimization of subgraphs, allows the calculation of a transfer function easier. In this work we repeat the mathematical methodology for the symbolic analysis of real electronic circuits on the basis of a given real circuitry. It is based on graph theory, the so called SFG method. To present the application we use a Common-X circuit as a use case. First, the Common-X circuit is split into its subcircuits and for each subcircuit it associated SFG is established. Then by the superposition of the SFGs of the subcircuits the total SFG for the Common-X circuit results.

2. Theoretical foundations

Signal flow graph: A signal-flow graph describes a system by its signal flows by directed and weighted graph (Samuel et al. 1956). Similarly, an SFG provides a graphical representation of a set of linear relationships (Brzozowski et al. 1963). For this reason, signal flow graph can be constructed between the materials using the Kirchhoff's laws the current and voltage relationship. The directed and undirected graphs, the signals are applied to nodes and functions on edges, the direction is given by an arrow on the edge. The nodes of the signal flow graphs are small processing units, through which the incoming signals are processed in a certain form. In this case, the result is sent to the outgoing edges (Richard et al. 2006). In network theory often are used ohmic resistors, capacitors and inductors. When considering these elements, the direction of the directed and weighted signal flow graph cannot be interchanged easily. Prior to changing the direction of the arrow direction, the function on the edge has to be inverted. The below material equation is shown as an example. The signal flow graph with the respective function on the edge is shown in Figure 1 (Fakhfakh et al. 2012).



Figure 1. SFG an ohmic resistance

Elements of a signal flow graph: A signal-flow graph exists next to edges and nodes of paths, loops, input node and output node. A node is a point or a circle, which reproduces a signal or a variable. Input node, also known as source node, has only outgoing paths and represent independent variables. An output node, also known as sink node, has only incoming paths and is in contrast to the input node a dependent variable. A path is a connected sequence of edges in one direction. The path gain is the product of the functions on the edges along a path. A reverse path is a path that leads towards the entrance node. A feedback loop is present when the start and end nodes are the same. Loops are equal oriented edges forming a closed path and will touch no node multiply. A self-referential loop is exactly present when a path flows from one node in the same node without crossing other nodes (Frieder et al. 2012).

Modifications of signal flow graph: By associative law sequential edges can be catenated (Figure 2). As soon as three nodes which are interconnected via a path so present, that there are the $x_0 \rightarrow x_1 \rightarrow x_2$ connected, the central node x_1 is eliminated from the graph:

 $x_0 \cdot a = x_1; x_1 \cdot b = x_2 \implies x_0 \cdot a \cdot b = x_2$

$$(x_0) \xrightarrow{a} (x_1) \xrightarrow{b} (x_2) = (x_0) \xrightarrow{ab} (x_2)$$

Figure 2: Summary sequential edges - associative law

Parallel running edges with the same input node x_0 and output node x_1 can be concatenated with the **distributive law** (Figure 3). The resulting graph is minimized to an edge. For example, two edges from node x_0 flow into the node x_1 . Algebraically, the node x_1 be expressed as:

 $x_0 \cdot a + x_0 \cdot b = x_0(a+b) = x_1$

$$x_0 \xrightarrow{a} x_1 = x_0 \xrightarrow{a+b} x_1$$

Figure 3: Summary of parallel edges – distributive law

Dissolving a feedback loop (Figure 4): In order to eliminate the node x_1 , be first the functions multiplied on the edges along the forward path. Next, forming the product of the individual loop gains. This is the signal-flow graph of two edges $a \cdot b$ and $b \cdot c$, in which $b \cdot c$ is a self-referential loop. Thus, the node x_1 is removed from the graph and the feedback has been summarized in a reflexive edge:

$$x_0 \cdot a = x_1 \text{ with } x_1 \cdot b = x_2 \implies x_0 \cdot a \cdot b + x_2 \cdot b \cdot c = x_2 \implies x_0 \cdot a \cdot b = x_2(1 - b \cdot c) \implies x_1 \frac{a \cdot b}{1 - b \cdot c} = x_2$$

$$(x_0 \xrightarrow{a} (x_1) \xrightarrow{c} (x_2) = (x_0 \xrightarrow{ab} (x_2) \xrightarrow{bc} (x_2) \xrightarrow{ab} (x_2) \xrightarrow{ab}$$

Figure 4: Dissolving a feedback loop

A reflexive edge (self-referential loop) can be eliminated, in which one by one divides the product of the functions on the

edges toward the reflective edge minus the product of the functions on the reflexive edges.

For more reflexive edges can use the same procedure. In Figure 5, the resolution reflexive edge is shown with the corresponding weights (Samuel et al. 1956, Brzozowski et al. 1963).



Figure 5: Dissolving a reflexive edge

3. Analysis of Common X-circuit

The Common X circuit (Figure 6) is chosen as an example of the determination of the signal flow graph in the course of work. Therefore, at this point the members of the small-signal model are explained:



Figure 6: Small signal equivalent circuit of the CX-circuit

 V_{in} is the input voltage, V_Z is the output voltage, R_Y is a lead resistance the internal resistance of the voltage source, r_p the baseband resistance of a BJT, g_m is the transconductance or the steepness of the CX circuit with $g_m = i_{out}/V_{in}$.

To apply now the method SFG, the circuit is divided into partial circuits. The intention in the division is to reduce the complexity of the analysis and to win by the sub-steps a better and clearer view of the functioning of the structure. The small-signal equivalent circuit diagram of the CX circuit can be divided into two parts following circuits: In order to simplify the effort of calculation, in the first step the circuit is broken. This results in two subcircuits (Figure 7). The first subcircuit is a simple voltage divider.



Figure 7: Small signal equivalent circuit of the CX-circuit in separate form

Based on the above considerations can now be derived for the first subcircuit of the signal-flow graph (Figure 8). It is desirable that the total voltage V_{in} of the voltage source drop across the resistor r_P . In reality, however, a small part of the voltage at the to much smaller resistance R_Y drops. The desired voltage at the resistor r_P can thus be adjusted with the resistance R_Y . Thus, the mesh equation for the first sub-circuit can be established: $V_P = V_{in} - V_{R_Y}$. Depending on the resistance r_P is generated by

 $V_P = V_{in} - V_{R_Y}$. Depending on the resistance V_P is generated by the voltage V_P of the current i_P . The material equation is: $i_P = V_P \cdot \frac{1}{r_P}$; $V_{R_Y} = i_Y \cdot R_Y$; $i_P = i_Y$.



Figure 8: First subcircuit (left) of the CX-circuit and SFG (right) of the first partial circuit



Figure 9: (Left) Second subcircuit of CX-circuit and (right) SFG of the second subcircuit

The current i_P flowing through the resistor R_Y and generates the voltage V_{R_Y} . Thus, the signal-flow graph of the first partial circuit may be formed by expansion of the signal flow graph of the ideal case without R_Y . This only needs around the edge (i_Y, V_{R_Y}) of the circuit to be supplemented. The dashed edges complement the axiomatic identity of the signal-flow graph.

When partitioning the common X-circuit, the second subcircuit between the nodes X and Z in Figure 6 is a current divider. In reality, not all of the current i of the source through the load resistor R_L :

$$i_{R_L} = i - i_{r_0}; i_{r_0} = V_0 \cdot \frac{1}{r_0}; V_L = V_0; V_L = i_{R_L} \cdot R_L.$$

Thus, the total current *i* can flowing through the load resistor R_L , the resistance r_0 would be infinite. But the resistance r_0 not infinitely large, flowing through it is a small portion of the source current.

The current i_{R_L} through the load resistor R_L can be adjusted by the appropriate choice of resistance r_0 or reduced by this resistance. Thus, the nodes usually can be placed. The current i_{R_L} generated at the load resistor R_L voltage V_L which is equal to the voltage drop across r_0 . With the mesh analysis, this relationship can be traced. The voltage across resistor r_0 generates the current i_{r_0} which acts back to the current i_{R_L} through a negative feedback. In summary, the node and mesh and the material equations for the second subcircuit can now be set up. Extending the signal flow graph of the simple circuit around the edge (V_0, i_{r_0}) of the circuit based on the above equations, then there is the signal flow graph of the second subcircuit. The material equations can be inverted. To make the signal flow graphs of CX-circuit, the individual subgraph must be combined into a graph.

The current source *i* is a voltage controlled current source. It is controlled by the voltage V_P . The current is determined by $i = g_m V_P$. In order for the two signal flow graph can about the relationship between the current source *i* and the voltage V_P interconnected (V_{in} (source), i_{R_I} (sink), i_P and V_L states).

4. Conclusion

The SFG analysis can offer a faster and more effective alternative to complex structures with the right approach and solution patterns. However, the signal-flow graph represents only a projection of the solution of the network equations. Superimposed by the inverted solution of the system all the states of the structure with self-imposed and unweighted loops are obtained. For the analysis of a network the SFG-method provides an important alternative, since you are saving in complex systems not only long calculus, but also get a suitable overview in the interaction of the system components and spare parts. The method is rarely used, and the existing literature on the subject is little. One can always encounter various problems in the analysis of a circuit that can be easily understood with the knowledge of this method and verified. The key to understanding a circuit is always their real structure, SFG is the structure faithful model, which real physics and underlying theory brings together suitable.



Figure 10: Signal flow graph of the CX-circuit for $r_P \rightarrow \infty$ *and* $R_L \square r_0$

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