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Research Article

Electrical characteristics of Au/Ti/HfO_2/*n*-GaAs metal-insulator-semiconductor structures with high-*k* interfacial layer

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ABSTRACT

We have fabricated, metal-insulator-semiconductor (MIS) structures, the Au/Ti/HfO2/*n*-GaAs. Metal rectifying contacts were made by DC magnetron sputtering technique, and hafnium dioxide (HfO2) interfacial insulating layer with 3, 5 and 10 nm thickness has been formed by the atomic layer depositon (ALD) technique. The series resistance values from the forward bias current-voltage (*I-V*) curves of 3 nm and 5 nm MIS structures has reduced very slightly with a decrease in the measurement temperature. The diode potential barrier height value from *I-V* characteristics increased with increasing HfO_2 layer thickness. Thus, the diode potential barrier height.was changed using the interfacial layer of the hafnium dioxide. Barrier height increment is an important and desirable feature in the field effect transistors (FET) and microwave mixers.

Keywords: Metal-oxide-semiconductor structures, GaAs semiconductor, Hafnia HfO_2, Atomic layer deposition (ALD) technique.

Yüksek *k*-arayüzey tabakalı metal-yalıtkan yarıiletken Au/Ti/HfO_2/*n*-GaAs yapıların Elektriksel Karakteristikleri

ÖZ

Au/Ti/HfO_2/*n*-GaAs metal-yalıtkan-yarıiletken (MIS) yapılar oluşturduk. Metal doğrultucu kontakları DC magnetron sputtering tekniğiyle yapıldı ve 3, 5 ve 10 nm kalınlıklı hafnium dioksit (HfO_2) arayüzey yalıtım tabakası atomic layer depositon (ALD) tekniğiyle oluşturuldu. 3 ve 5 nm MIS diyotların doğru besleme akım-gerilim eğrilerinden seri direnç değerleri, ölçüm sıcaklığındaki bir azalma ile çok hafif bir şekilde azaldı. *I-V* karakteristiklerinden diyot potansiyel engel yüksekliği değeri artan HfO_2 tabaka kalınlığıyla arttı. Böylece, hafnium dioksit arayüzey tabakası kullanılarak diyot potansiyel engel yüksekliği değiştirildi. Bariyer yükseklik artırma, alan etkili transistörler (FET) ve mikrodalga karıştırıcılarında önemli ve istenen bir özelliktir.

Anahtar Kelimeler: Metal-oksit-yarıiletken yapılar, GaAs yarıiletkeni, Hafnia HfO_2, Atomic tabakalı depolama (ALD) tekniği.

1. INTRODUCTION

The Metal-semiconductor (MS) rectifying and ohmic contacts are of huge importance in fabricating modern electronic device applications such as bipolar transistor, field effect transistor (FET) and metal-oxide-semiconductor (MOS) FET (i.e. MOSFET). MS rectifying current and admittance theory serve in understanding the foundation of the semiconductor device physics.[1-6] The metal-insulator-semiconductor (MIS) or MOS capacitors are the most useful devices in semiconductor surface physics studies since most practical problems in the reliability and stability of all semiconductor devices are closely related to their surface

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conditions.[1-10] We have prepared the Au/Ti/HfO_2/*n*-GaAs MIS structures. The metal oxide interfacial layer with 3, 5 and 10 nm thickness, the hafnium dioxide (HfO_2) thin film, was grown by the ALD technique. Ti (10 nm) Schottky contacts have been produced on HfO_2/*n*-GaAs structure by DC magnetron sputtering technique, and Au (50 nm) was evaporated as a top layer on the Ti/*n*-GaAs structure under 10^{-6} Torr vacuum. We have described the current-voltage (*I-V-T*) characteristics of these MIS diodes.

Hafnium oxide (HfO_2) known as hafnia is a colourless solid and is an inorganic insulating compound. Also, HfO_2 is one of the most common and stable compounds of hafnium. It is a material with high dielectric constant, i.e. high-*k* dielectric. As it is well-known, the insulating or oxide interfacial layer is one of the most critical MOSFET components. It is an electrical insulator with a band gap of nearly 6 eV and a high dielectric constant value of 22, which is utilized to increase the interfacial layer capacitance without generating excess gate current in a MOSFET and thus to achieve a large current.[1,4-10] Therefore, the oxide film growth technique is a very important issue. The ALD technique is one of the most important methods for preparing high quality high-*k* dielectric thin metal-oxide layers. The layer-by-layer nature of the deposition kinetics of the ALD process allows surface-controlled nearly perfect thin films with excellent electrical characteristics.[5-10]

Generally, the SiO_2 is the main dielectric gate oxide material in the semiconductor electronic industry owing to its excellent compatibility with Si semiconductors. However, the main disadvantage of SiO_2 is its high power consumption and large leakage currents which limits its technological applications. For instance, the improved performance of complementary CMOS transistors requires the high k-metal oxides such as HfO_2 the substitution of the SiO_2 gate oxide.[4-7] Therefore, the high k-metal oxides such as HfO_2 can be selected for the GaAs MOSFETs, MOS high-electron-mobility transistors (MOS-HEMTs) and high voltage power switching devices.[5-10]

2. EXPERIMENTAL PROCEDURES

The Au/Ti/HfO_2/*n*-GaAs structures were produced utilizing *n*-type GaAs wafer with (100) crystal orientation, having 300 µm thickness, 2 inch diameter and 1.2 Ω cm resistivity (the manufacturer data) and 6.8 x 1015 cm^{-3} carrier concentration. Before the SBD fabrication process, the experimental procedure was first performed by a cleaning procedure which is sonicated for 2 minutes in aceton and prophanol, and then rinsed in deionized water thoroughly and dried under nitrogen gas flow. After cleaning of n-GaAs's surface, Indium metal (purity of 99.999%) which has a thickness of nearly 2000 Å was deposited for back-side ohmic contact at a reactor pressure approximately 10^{-6} Torr in a high-vacuum thermal evaporation system. In order to form the low-resistance ohmic contact, In-deposited n-GaAs wafer was annealed at 385°C for 3 min under the nitrogen gas atmosphere. After this process, HfO_2 thin films were deposited on the cleaned top surface of GaAs samples using standard thermal ALD system (Savannah S100 ALD reactor, Cambridge Nanotech Inc.). Deposition was carried out at 200°C using tetrakis (dimethylamido hafnium [$Hf(NMe_2)_4$] and water (H_2O) as the organometallic precursor and oxygen source, respectively. $Hf(NMe_2)_4$ was preheated to 75°C and stabilized at this temperature before the deposition. Carrier gas (N_2) with a flow rate of 20 sscm was utilized. Pulse times of the Hf precursor and oxygen source were 0.2 and 0.015 s, respectively. Purging was done after each step. Deposition rate for this recipe was determined about 1 Å per cycle. The total number of ALD cycles was used to precisely control the thickness of deposited hafnia layer. Afterwards, for Schottky diode fabrication, the hafnia coated and Indium-back-contacted GaAs sample was patterned via standard lithography process. After development process, the sample was rinsed entirely in de-ionized water. On the top of the ALD-grown HfO_2 insulating layer, Au (90nm)/Ti(10nm) Schottky contacts were formed using DC magnetron sputtering technique. Figure 1 shows the schematical representation of experimentally produced MIS devices.

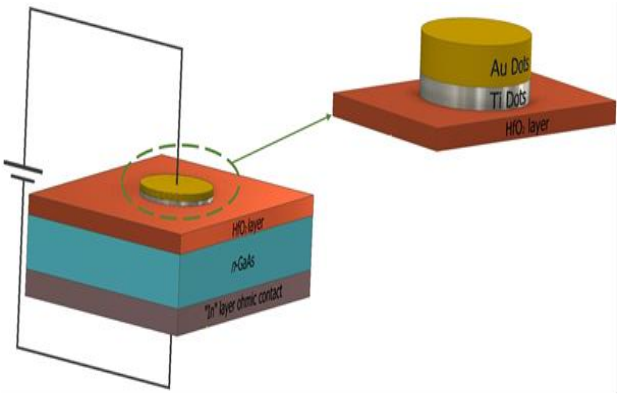

Figure 1. Schematical representation of experimentally produced MIS devices.

After fabrication process, the current-sample temperature-voltage (*I-T-V*) characteristics were measured using a Leybold Heraeus closed-cycle helium cryostat and a Keithley 487 Picoammeter Voltage Source in dark conditions. The sample temperature was always monitored by a copper-constantan thermocouple and by a Windaus MD850 electronic thermometer which has better sensitivity than ± 0.1 K.

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3. RESULTS AND DISCUSSION

Figure 2 illustrates 3D for the surface morphology of deposited 3 nm HfO_2 on substrate, the RMS value is 1.09 nm. Figure 3 shows 3D for the surface morphology of deposited 5 nm HfO_2 on substrate, the RMS value is 1.20 nm. Figure 4 shows 3D f or the surface morphology of deposited 10 nm HfO_2 on *n*-type GaAs substrate, the RMS value is 1.19 nm.

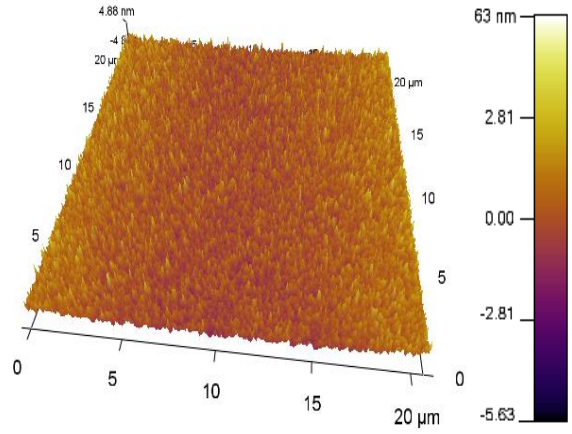

Figure 2. 3D for the surface morphology of 3 nm HfO_2 deposited on *n*-GaAs substrate, the RMS value is 1.09 nm.

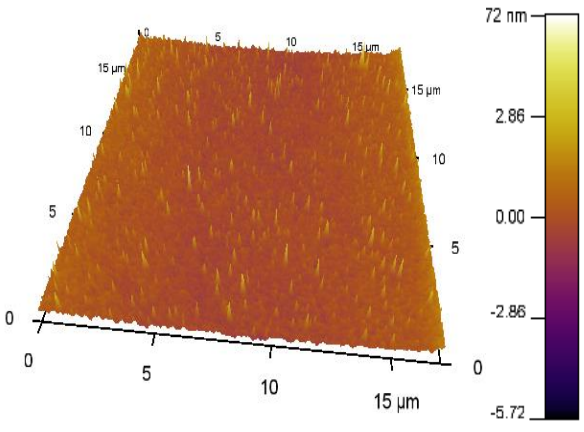

Figure 3. 3D for the surface morphology of 5 nm HfO_2 deposited on *n*-GaAs substrate, the RMS value is 1.20 nm.

The experimental *I-V* characteristics at 60, 200, 300 and 400 K of the MIS diodes structures are given in Figures 5 and 6. The current by the carriers across the diode is supplied by the thermionic emission (TE) given in Eq. (1).[1-4]

$$I = I_0\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (1)$$

where I_0 indicates the saturation current, and it is expressed by Eq. (2).

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \quad (2)$$

Φ_{b0} and n indicate the effective barrier height (BH) at zero bias and ideality factor calculated from the intercept and slope of the linear portion of the semi-log forward bias ln*I-V* characteristics, respectively. A^* showes the effective Richardson constant of 8.16 $Acm^{-2}K^{-2}$ for *n*-type GaAs. A is the diode area. R_S indicates the series resistance from the neutral region of the semiconductor substrate and the interfacial layer HfO_2. The IR_S is the voltage drop across the series resistance, respectively.[12-24] The R_S value was calculated using Cheung's method arranged from Eq. (1).[11]

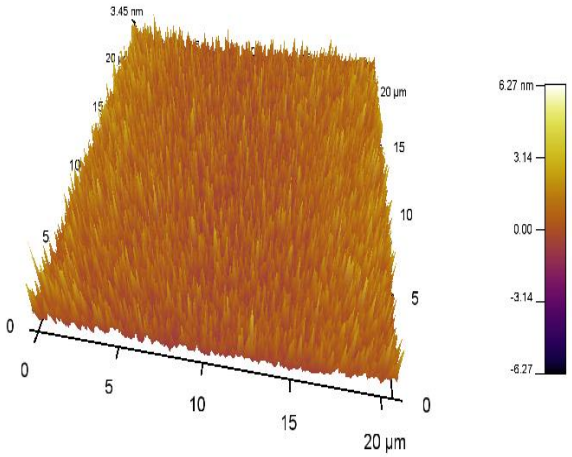

Figure 4. 3D for the surface morphology of 10 nm HfO_2 deposited on *n*-type GaAs substrate, the RMS value is 1.19 nm.

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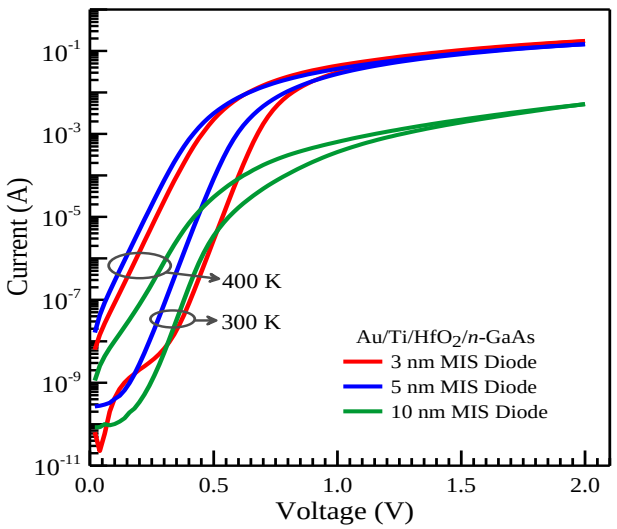

Figure 5. Experimental forward bias *I-V* characteristics for MIS structures with 3, 5 and 10 nm HfO_2 interfacial layer thicknesses at 300 and 400 K.

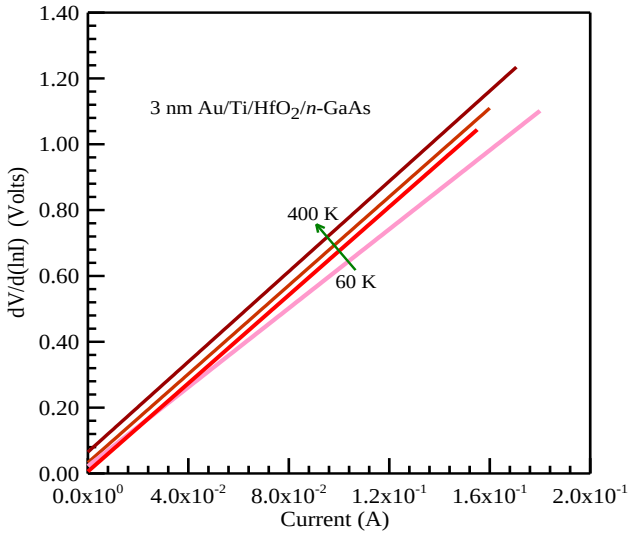

Figure 7. dV/d(lnI) versus current plots by Cheung's Model for determining the series resistance for the 3 nm MIS diode at different temperatures.

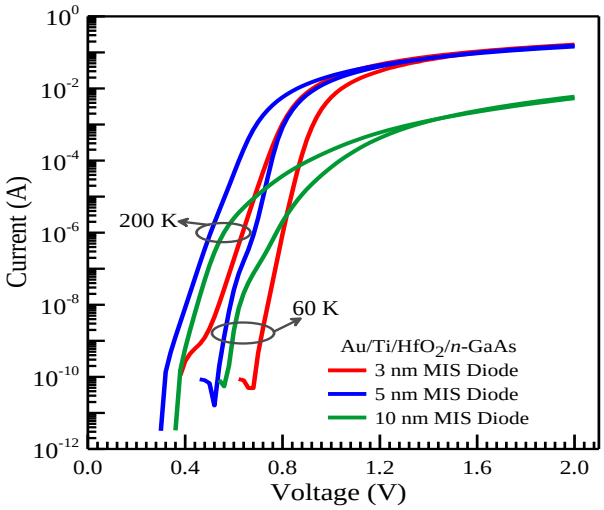

Figure 6. Experimental forward bias *I-V* characteristics at 60 and 200 K for the MIS structures with 3, 5 and 10 nm HfO_2 interfacial layer thicknes.

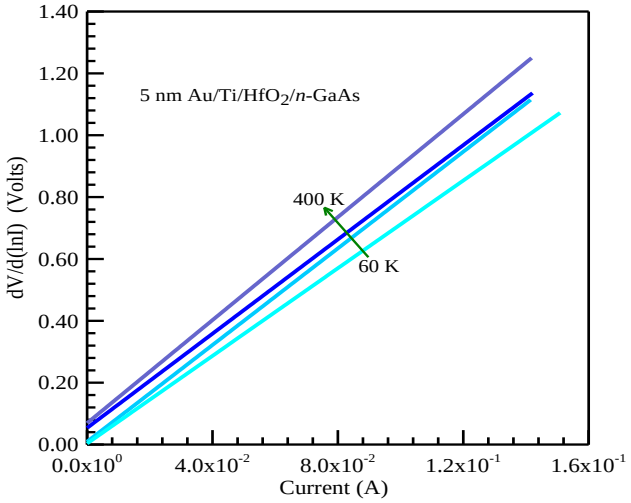

Figure 8. dV/d(lnI) versus current plots by Cheung's Model for determining the series resistance at different temperatures for the MIS structure with 5nm HfO_2 interfacial layer thickness.

The plots by Cheung's method are given in Figures 7, 8 and 9. The calculated R_S, Φ_{b0} and n values for the diodes are given in Table 1. The R_S value for the MIS diodes of 3 and 5 nm very has slightly reduced from 60 K to 400 K, and ranged from 7.26 Ω at 400 K to 6.30 Ω and 60 K for the MIS diode of 3 nm and from 8.33 Ω to 7.10 Ω for the MIS diode of 5 nm and from 166 Ω to 111 Ω for 10 nm MIS diode, respectively. This extreme value for the MIS diode of 10 nm comes from the contribution of the HfO_2 interfacial layer and imperfect ohmic contact to the semiconductor substrate.[12-24]

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Table 1. The experimental parameters from the forward bias *I-V* characteristics at some measurement temperatures for the MIS diodes with different HfO_2 interfacial layer thickness fabricated by us

T (K)	3 nm Au/Ti/*n*-GaAs			5 nm Au/Ti//HfO_2/*n*-GaAs			10 nm Au/Ti//HfO_2/*n*-GaAs		
	n	Φ_b (eV)	R_S (Ω)	*n*	Φ_b (eV)	R_S (Ω)	*n*	Φ_b (eV)	R_S (Ω)
400	1.03	0.99	7.26	1.04	0.94	8.33	1.20	1.06	166
300	1.09	1.02	6.76	1.09	0.93	7.98	1.06	1.00	138
200	1.25	0.89	6.70	1.24	0.78	7.81	2.20	0.90	126
60	2.72	0.40	6.30	2.58	0.37	7.10	6.88	0.20	111

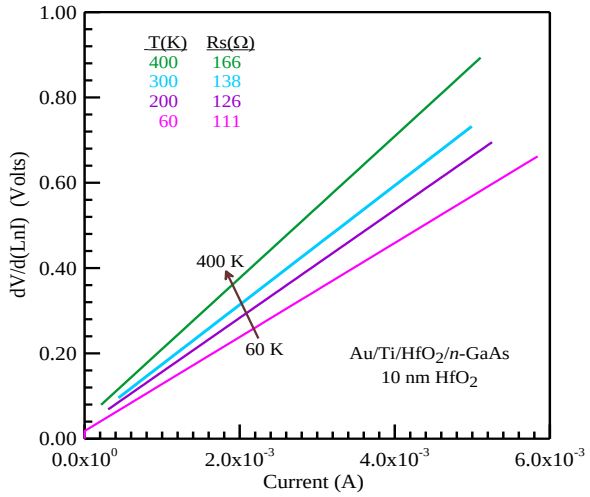

Figure 9. dV/d(lnI) versus current plots by Cheung's Model for determining the series resistance at different temperatures for the MIS structure with 10 nm HfO_2 interfacial layer thickness.

This behavior of the R_S in high-bias region arises from strongly dependent on the semiconductor substrate mobility increasing with an increase in temperature.[25,26] Similarly, Osvald and Horvath[26] have resulted from the theoretical study of the temperature dependence of Schottky diodes that the cross-point independent of measurement temperature at certain voltage depends on the doping concentrations and thickness of the doped near-surface layer of semiconductor substrate.

The BH Φ_{b0} and *n* calculated using Equations (1) and (2) are provide to understand the contribution from other current mechanisms through the devices such as generation recombination and tunneling. The additional contributions other than TE can cause significant deviation in the extraction of these characteristic parameters.[8,27]

As seen in Table 1, the BH decreased with a decrease in the temperature because the current preferentially flows through the lowest BH with a decrease in temperature due to the BH inhomogeneity.[27-35] It can be seen from Figures 6 and 7 that the current value of the 5 nm MIS diode at a given bias is larger than that of the MIS diode of 3 nm up to the starting point of the downward curvature region of the *I-V* curve for all temperatures. The use of very thin interfacial layer increases the interfacial layer capacitance without generating excess gate current in a MOSFET and thus causes a large current through device.[1,4-10]

As seen in Table 1, the BH values for the MIS diode of 3 nm range from 0.99 eV at 400 and 0.40 eV at 60 K, and *n* values range from 1.03 at 400 and 2.72 at 60 K. The BH values for the 5 nm MIS diode range from 0.94 eV at 400 and 0.37 eV at 60 K, and *n* values range from 1.04 at 400 and 2.58 at 60 K. Moreover, the BH values for the 10 nm MIS diode range from 1.06 eV at 400 and 0.20 eV at 60 K, and *n* values range from 1.20 at 400 and 6.88 at 60 K. The BH and the *n* values for the 10 nm MIS diode at 400 K are larger than those for the other two diodes. It can be said that the case is supplied from the more thickness interfacial layer. An increased high barrier height-diode is useful for the gates of MESFETs and can supply a sufficient barrier height for FET operation and be used in the microwave rectifier applications with the DC offset voltage.[3-10,35] As can be seen from Figures 5 and 6, the reducing the diode current, the additional barrier increasing and the non-ideality in the forward bias *I-V* characteristics for the 10 nm MIS diode comes from the interface state charge change and the potential change across the interfacial layer as a result of the voltage applied.[1-4,36]

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4. CONCLUSIONS

The value of R_S has decreased with a decrease in the temperature. It has been expressed that this behavior of the series resistance arises from strongly dependent on the semiconductor substrate mobility increasing with an increase in temperature and the thickness of the counter-doped near-surface layer of semiconductor substrate. The increase in the BH due to insulating layer between metal-GaAs substrate is useful for the gates of MESFETs and can provide an adequate BH for FET operation and be used in the microwave rectifier applications with the DC offset voltage.

Conflict of interest

We declare that there is no a conflict of interest with any person, institute, company, etc.

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